LibreSilicon Standard Cell Library

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Abstract

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For further clarification consult the complete documentation of the process.

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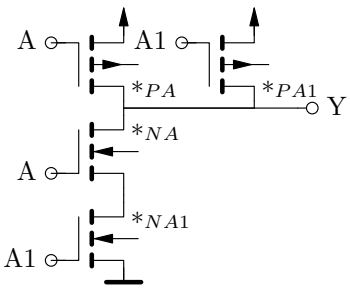
1 Considerations

2 Logical Cells

3 Cell AOI21

Schematic (one stage, $1T_p/2T_n$ stacked, $4T$ total)



4 Cell ASYNC1

Schematic (one stage, $2T_p/2T_n$ stacked, $12T$ total)

5 Cell ASYNC2

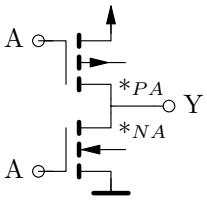
Schematic (one stage, $2T_p/2T_n$ stacked, $8T$ total)

6 Cell ASYNC3

Schematic (one stage, $3T_p/3T_n$ stacked, $12T$ total)

7 Cell INV

Schematic (one stage, $1T_p/1T_n$ stacked, $17T$ total)

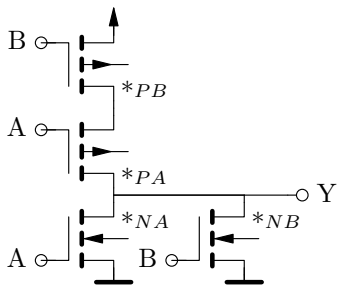


8 Cell martin1989

Schematic (one stage, $2T_p/2T_n$ stacked, $8T$ total)

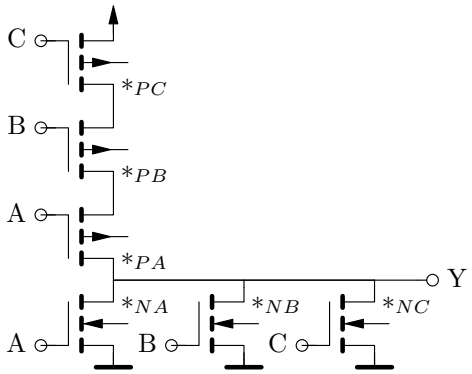
9 Cell NOR2

Schematic (one stage, $2T_p/1T_n$ stacked, $4T$ total)



10 Cell NOR3

Schematic (one stage, $3T_p/1T_n$ stacked, $6T$ total)



11 Cell sutherland1989

Schematic (one stage, $2T_p/2T_n$ stacked, $12T$ total)

12 Cell vanberkel1991

Schematic (one stage, $3T_p/3T_n$ stacked, $12T$ total)

VDDIO
GND
ANA