

# LibreSilicon Standard Cell Library

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## **Abstract**

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For further clarification consult the complete documentation of the process.

# Contents

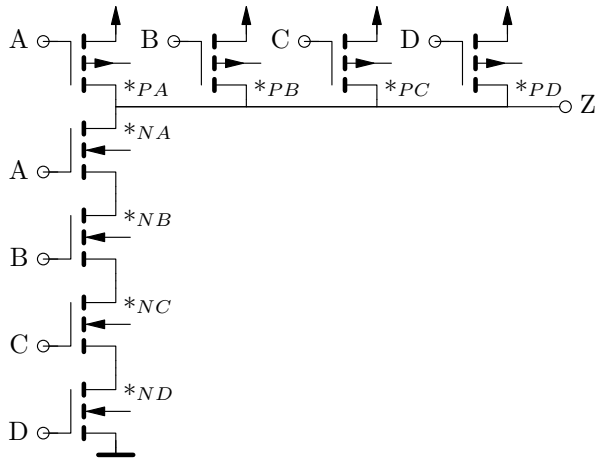
1	Considerations	3
2	Logical Cells	4
3	Cell AND4	5
4	Cell AOI21	6
5	Cell AOI31	7
6	Cell BUFX2	8
7	Cell BUFX4	9
8	Cell FILL	10
9	Cell INV	11
10	Cell INVX1	12
11	Cell INVX2	13
12	Cell INVX4	14
13	Cell INVX8	15
14	Cell MUX2X1	16
15	Cell NAND2	17
16	Cell NAND2X1	18
17	Cell NAND3	19
18	Cell NAND3X1	20
19	Cell NOR2	21
20	Cell NOR2X1	22
21	Cell NOR3	23
22	Cell OAI21	24
23	Cell OAI31	25
24	Cell OR4	26
25	Cell TBUFX1	27
26	Cell XNOR2X1	28
27	Cell XOR2X1	29

# 1 Considerations

## 2 Logical Cells

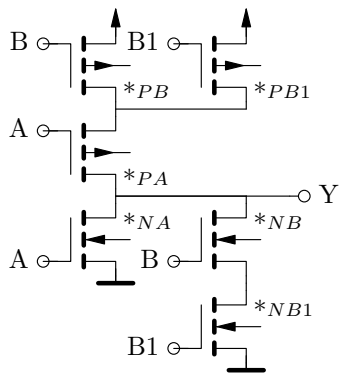
### 3 Cell AND4

Schematic (two stage,  $1T_p/4T_n$  stacked,  $10T$  total)



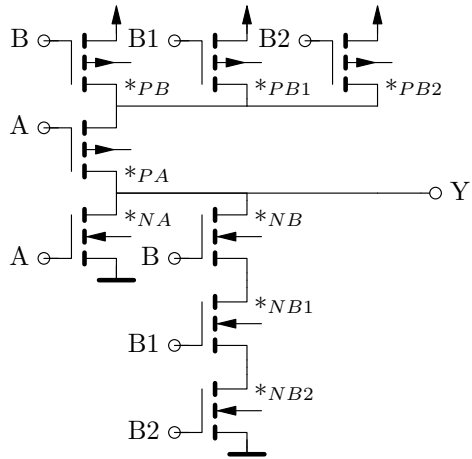
## 4 Cell AOI21

Schematic (one stage,  $2T_p/2T_n$  stacked,  $6T$  total)



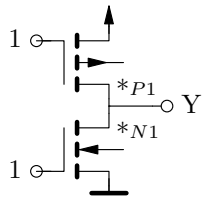
## 5 Cell AOI31

Schematic (one stage,  $2T_p/3T_n$  stacked,  $8T$  total)



## 6 Cell BUFEX2

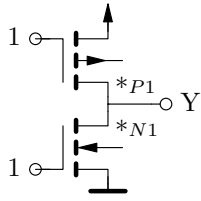
Schematic (one stage,  $1T_p/1T_n$  stacked,  $4T$  total)





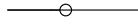
## 7 Cell BUFX4

Schematic (one stage,  $1T_p/1T_n$  stacked,  $6T$  total)



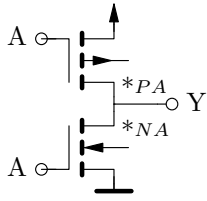
## 8 Cell FILL

Schematic (one stage,  $0T_p/0T_n$  stacked,  $0T$  total)



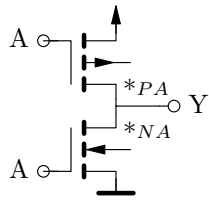
## 9 Cell INV

Schematic (one stage,  $1T_p/1T_n$  stacked,  $17T$  total)



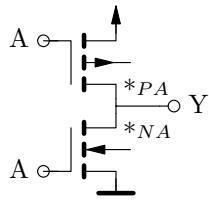
## 10 Cell INVX1

Schematic (one stage,  $1T_p/1T_n$  stacked,  $2T$  total)



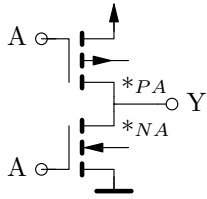
## 11 Cell INVX2

Schematic (one stage,  $1T_p/1T_n$  stacked,  $2T$  total)



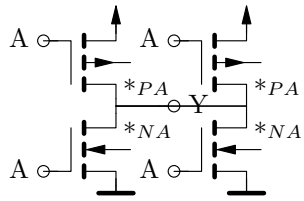
## 12 Cell INVX4

Schematic (one stage,  $1T_p/1T_n$  stacked,  $4T$  total)



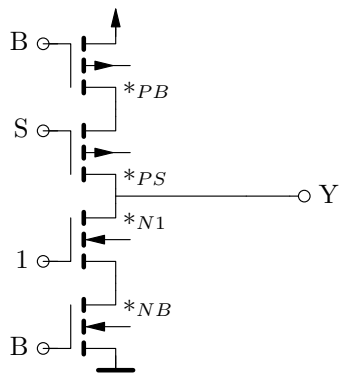
### 13 Cell INVX8

Schematic (one stage,  $1T_p/1T_n$  stacked,  $8T$  total)



## 14 Cell MUX2X1

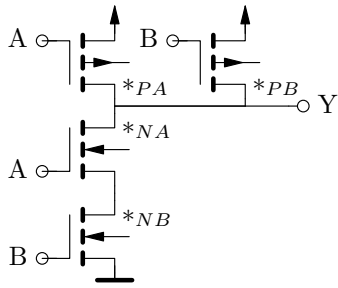
Schematic (one stage,  $2T_p/2T_n$  stacked,  $10T$  total)





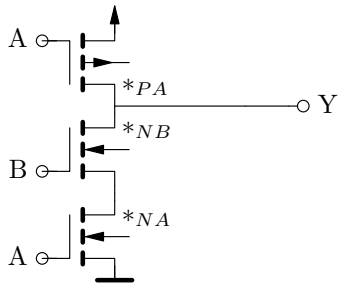
## 15 Cell NAND2

Schematic (one stage,  $1T_p/2T_n$  stacked,  $4T$  total)



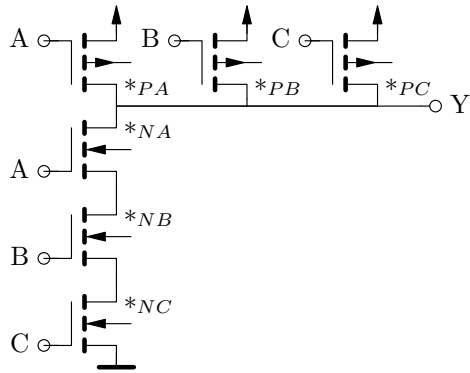
## 16 Cell NAND2X1

Schematic (one stage,  $1T_p/2T_n$  stacked,  $4T$  total)



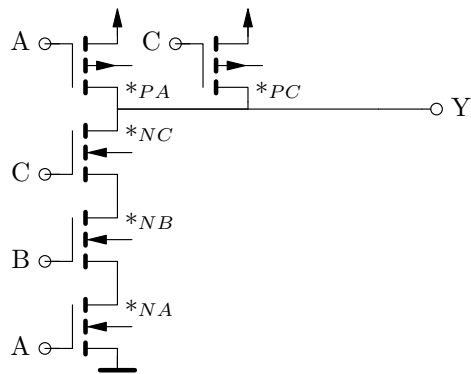
## 17 Cell NAND3

Schematic (one stage,  $1T_p/3T_n$  stacked,  $6T$  total)



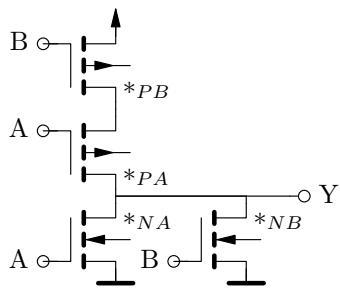
## 18 Cell NAND3X1

Schematic (one stage,  $1T_p/3T_n$  stacked,  $6T$  total)



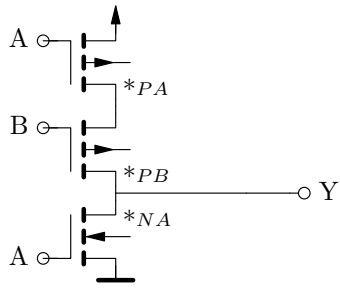
## 19 Cell NOR2

Schematic (one stage,  $2T_p/1T_n$  stacked,  $4T$  total)



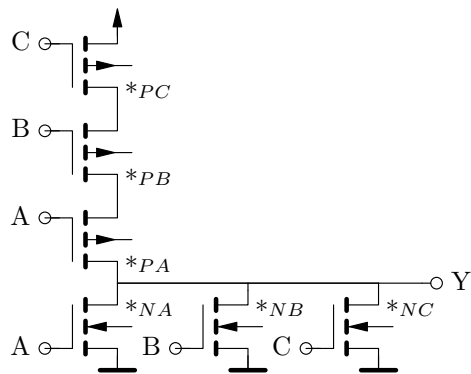
## 20 Cell NOR2X1

Schematic (one stage,  $2T_p/1T_n$  stacked,  $4T$  total)



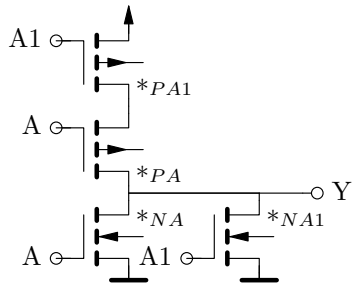
## 21 Cell NOR3

Schematic (one stage,  $3T_p/1T_n$  stacked,  $6T$  total)



## 22 Cell OAI21

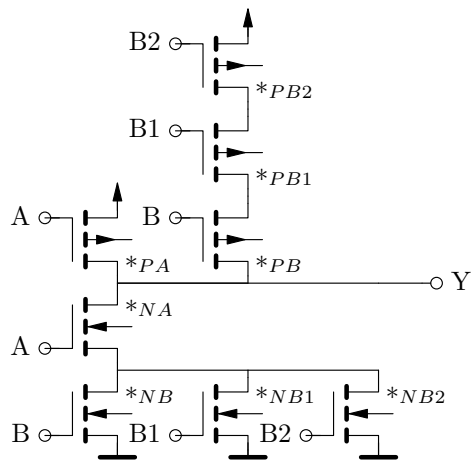
Schematic (one stage,  $2T_p/1T_n$  stacked,  $4T$  total)





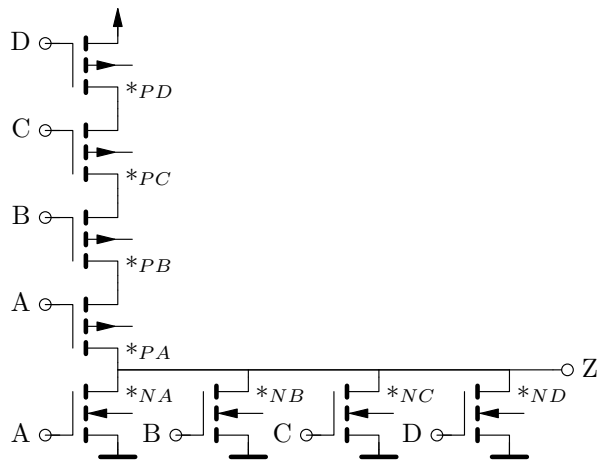
## 23 Cell OAI31

Schematic (one stage,  $3T_p/2T_n$  stacked,  $8T$  total)



## 24 Cell OR4

Schematic (two stage,  $4T_p/1T_n$  stacked,  $10T$  total)



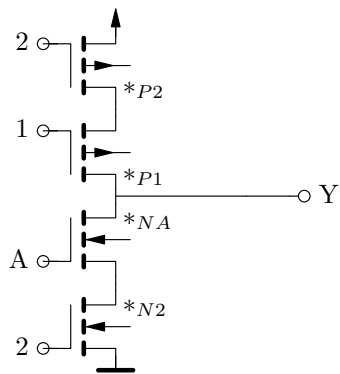
## 25 Cell TBUF<sub>X1</sub>

Schematic (one stage,  $1T_p/1T_n$  stacked,  $6T$  total)

—○ vdd

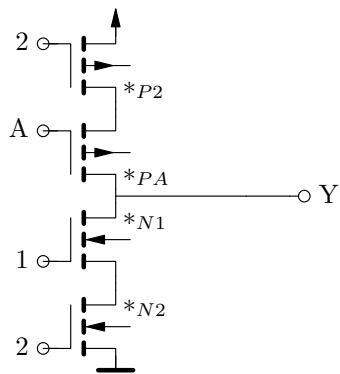
## 26 Cell XNOR2X1

Schematic (one stage,  $2T_p/2T_n$  stacked,  $12T$  total)



## 27 Cell XOR2X1

Schematic (one stage,  $2T_p/2T_n$  stacked,  $12T$  total)



VDDIO  
GND  
ANA

