LibreSilicon's Standard Cell Library

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Abstract

Document Revision History

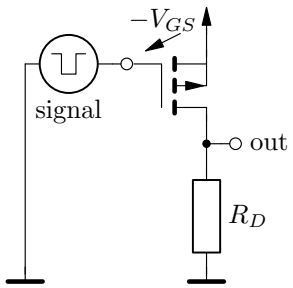
VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-02-01	START with empty document, ADD many cells	-

Contents

1 CMOS in a nutshell

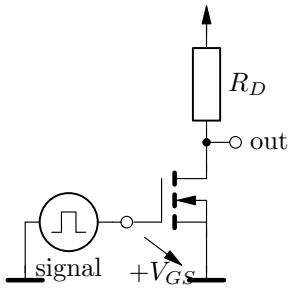
This basic initial project is dedicated to the CMOS Technology only and for this reason two types of metal--oxide-semiconductor field-effect transistors (MOSFET) are required.
Historicaly, the first chips with MOSFETs on the mass market were p-channel MOSFETs in enhancement-mode.

enhancement-mode PMOS transistor use-case



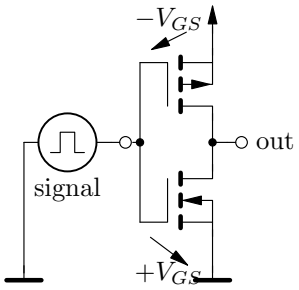
The sectional view of a PMOS transistor in silicon is being shown below
Historicaly later, faster chips with MOSFETs on the mass market were marked as n-channel MOSFETs in enhancement mode also.

enhancement-mode NMOS transistor use-case



The sectional view of a NMOS transistor in silicon is being shown here also.
Both technologies, the older NMOS as the newer PMOS, have the same disadvantage. Every time, the transistor is switched on, the current between Drain and Source of the transistor is limited by the Resistor on Drain only. Higher currents here meaning higher power consumption for the chip where the transistors are integrated also. If the transistors are switched off, no currents flows between Drain and Source anymore, the power consumption of the chip also goes low.
Et violà, the US-Patent with Number 3356858[1]changed the world and combines both technologies to the new complementary metal-oxide-semiconductor (CMOS) technology. Instead of every transistor is working against a weak resistor, the transistor works against a complementary switched-off transistor. With the Eyes of our antecessor CMOS doubles the transistor count, but contemporary chips all are build in CMOS.

complementary PMOS and NMOS transistor couple use-case



The sectional view of a NMOS and PMOS transistors couple in silicon - building the CMOS technology - are being shown here also.

[1] https://www.google.com/patents/US3356858

2 Logical Cells

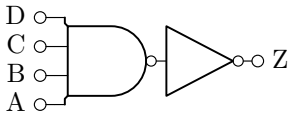
2.1 AND4 - a 4-input AND gate

Synopsys

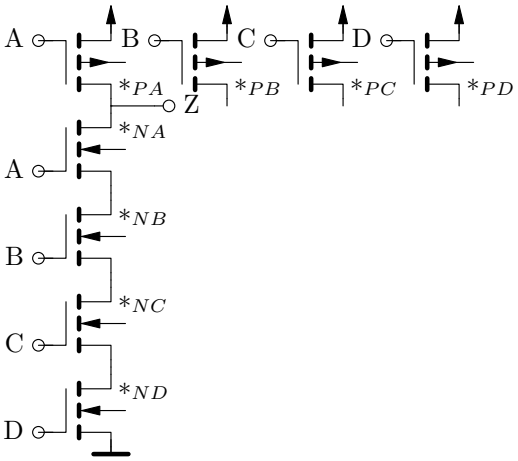
AND4 (Z Y Y D C B A)

Description

Circuit



Schematic (one stage, $1T_p/4T_n$ stacked, $10T$ total)



Truth Table

$$Z = D \cdot C \cdot B \cdot A$$

D	C	B	A	Z
0	X	X	X	0
X	0	X	X	0
X	X	0	X	0
X	X	X	0	0
1	1	1	1	1

Usage

Fan-in / Fan-out

Layout

Files

See also

NAND3 - a 3-input Not-AND (or NAND) gate

Cell

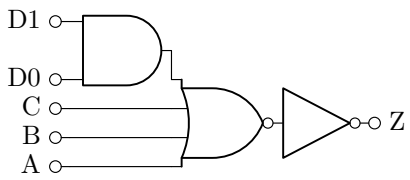
AO2111 - a 2-1-1-1-input AND-OR gate

Synopsys

AO2111(Z, D1, D0, C, B, A)

Description

Circuit



Truth Table

$$Z = (D1 \wedge D0) \vee C \vee B \vee A$$

D1	D0	C	B	A	Z
0	X	0	0	0	0
0	X	1	X	X	1
0	X	X	1	X	1
0	X	X	X	1	1
X	0	0	0	0	0
X	0	1	X	X	1
X	0	X	1	X	1
X	0	X	X	1	1
1	1	X	X	X	1

Usage

Fan-in / Fan-out

Layout

Files

See also

AO3111 - a 3-1-1-1-input AND-OR gate

Cell

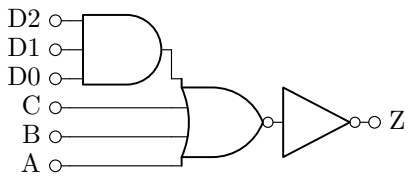
AO3111 - a 3-1-1-1-input AND-OR gate

Synopsys

AO3111(Z, D2, D1, D0, C, B, A)

Description

Circuit



D2	D1	D0	C	B	A	Z
0	X	X	0	0	0	0
0	X	X	1	X	X	1
0	X	X	X	1	X	1
0	X	X	X	X	1	1
X	0	X	0	0	0	0
X	0	X	1	X	X	1
X	0	X	X	1	X	1
X	0	X	X	X	1	1
X	X	0	0	0	0	0
X	X	0	1	X	X	1
X	X	0	X	1	X	1
X	X	0	X	X	1	1
1	1	1	X	X	X	1

Truth Table

$$Z = (D2 \wedge D1 \wedge D0) \vee C \vee B \vee A$$

Usage

Fan-in / Fan-out

Layout

Files

See also

AO2111 - a 2-1-1-1-input AND-OR gate

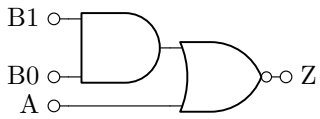
2.2 AOI21 - a 2-1-input AND-OR-Invert gate

Synopsys

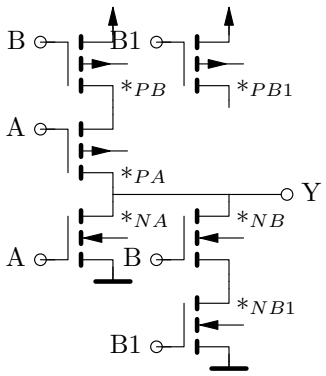
AOI21 (Y B1 B A)

Description

Circuit



Schematic (one stage, $2T_p/2T_n$ stacked, $6T$ total)



Truth Table

$$Z = \neg((B1 \wedge B0) \vee A)$$

B1	B0	A	Z
0	X	0	1
1	1	X	0
X	0	0	1
X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI31 - a 3-1-input AND-OR-Invert gate

Cell

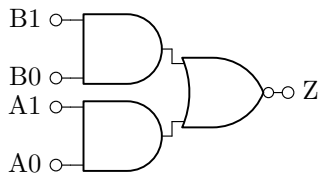
AOI22 - a 2-2-input AND-OR-Invert gate

Synopsys

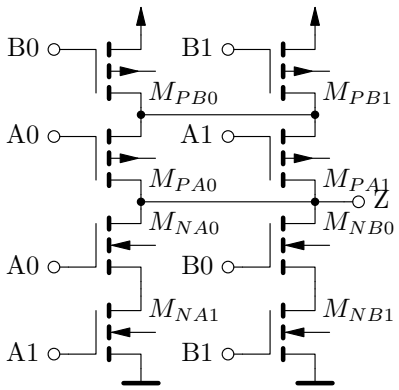
AOI22(Z, B1, B0, A1, A0)

Description

Circuit



Schematic (one stage, $2T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((B1 \wedge B0) \vee (A1 \wedge A0))$$

B1	B0	A1	A0	Z
0	X	0	X	1
0	X	X	0	1
1	1	X	X	0
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI33 - a 3-3-input AND-OR-Invert gate

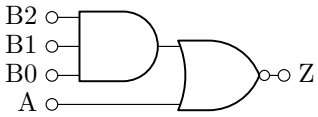
2.3 AOI31 - a 3-1-input AND-OR-Invert gate

Synopsys

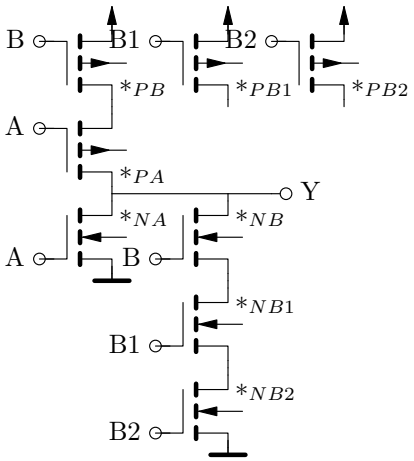
AOI31 (Y B2 B1 B A)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, $8T$ total)



Truth Table

$Z = \neg((B2 \wedge B1 \wedge B0) \vee A)$

B2	B1	B0	A	Z
0	X	X	0	1
1	1	1	X	0
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI21 - a 2-1-input AND-OR-Invert gate

Cell

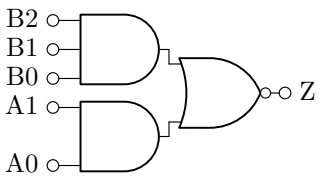
AOI32 - a 3-2-input AND-OR-Invert gate

Synopsys

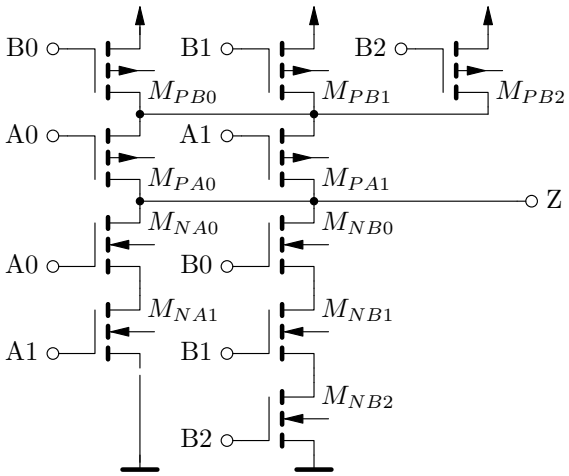
AOI32(Z, B2, B1, B0, A1, A0)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((B2 \wedge B1 \wedge B0) \vee (A1 \wedge A0))$$

B2	B1	B0	A1	A0	Z
0	X	X	0	X	1
0	X	X	X	0	1
1	1	1	X	X	0
X	0	X	0	X	1
X	0	X	X	0	1
X	X	0	0	X	1
X	X	0	X	0	1
X	X	X	1	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI22 - a 2-2-input AND-OR-Invert gate
AOI33 - a 3-3-input AND-OR-Invert gate

Cell

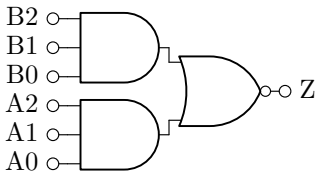
AOI33 - a 3-3-input AND-OR-Invert gate

Synopsys

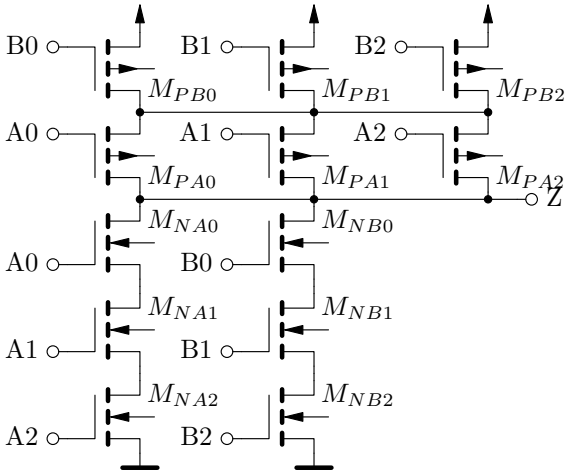
AOI33(Z, B2, B1, B0, A2, A1, A0)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 12T total)



Truth Table

$$Z = \neg((B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$$

Usage

Fan-in / Fan-out

Layout

Files

B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	1
0	X	X	X	0	X	1
0	X	X	X	X	0	1
1	1	1	X	X	X	0
X	0	X	0	X	X	1
X	0	X	X	0	X	1
X	0	X	X	X	0	1
X	X	0	0	X	X	1
X	X	0	X	0	X	1
X	X	0	X	X	0	1
X	X	X	1	1	1	0

See also

AOI22 - a 2-2-input AND-OR-Invert gate
AOI32 - a 3-2-input AND-OR-Invert gate

Cell

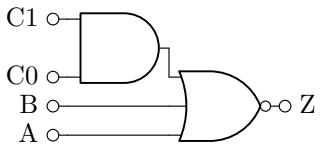
AOI211 - a 2-1-1-input AND-OR-Invert gate

Synopsys

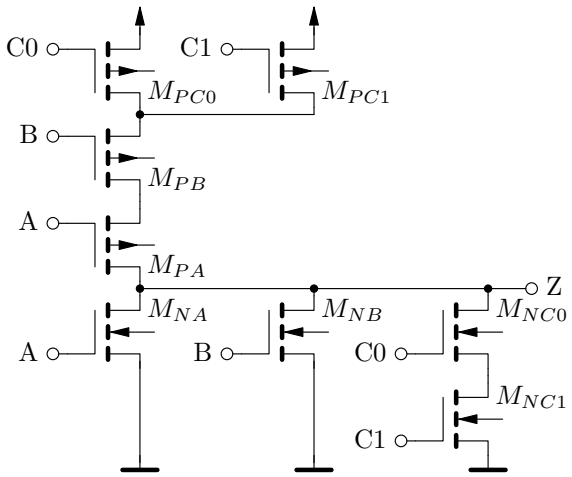
AOI211(Z, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((C1 \wedge C0) \vee B \vee A)$$

C1	C0	B	A	Z
0	X	0	0	1
1	1	X	X	0
X	0	0	0	1
X	X	1	X	0
X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI311 - a 3-1-1-input AND-OR-Invert gate

Cell

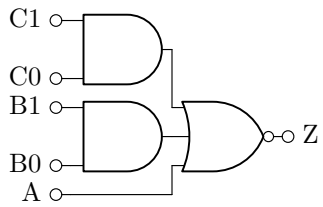
AOI221 - a 2-2-1-input AND-OR-Invert gate

Synopsys

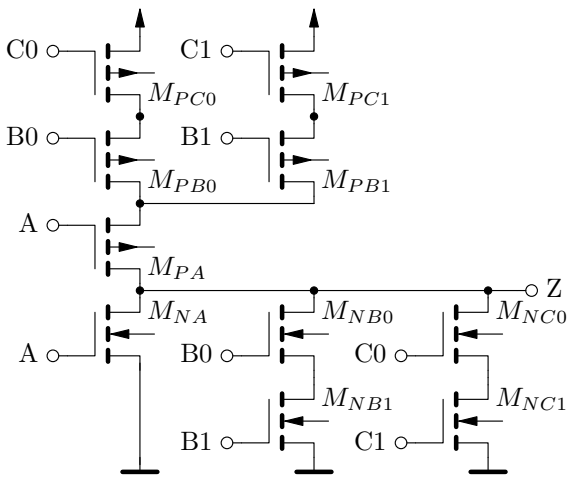
AOI221(Z, C1, C0, B1, B0, A)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C1 \wedge C0) \vee (B1 \wedge B0) \vee A)$$

C1	C0	B1	B0	A	Z
0	X	0	X	0	1
0	X	X	0	0	1
1	1	X	X	X	0
X	0	0	X	0	1
X	0	X	0	0	1
X	X	1	1	X	0
X	X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI321 - a 3-2-1-input AND-OR-Invert gate
AOI331 - a 3-3-1-input AND-OR-Invert gate

Cell

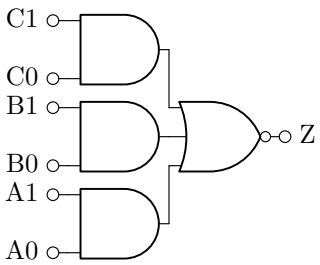
AOI222 - a 2-2-2-input AND-OR-Invert gate

Synopsys

AOI222(Z, C1, C0, B1, B0, A1, A0)

Description

Circuit



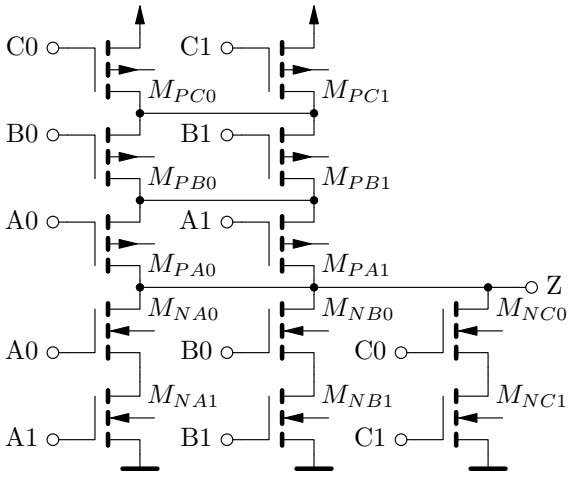
Schematic (one stage, $3T_p/2T_n$ stacked, 12T total)

Truth Table

$$Z = \neg((C1 \wedge C0) \vee (B1 \wedge B0) \vee (A1 \wedge A0))$$

Usage

Fan-in / Fan-out



C1	C0	B1	B0	A1	A0	Z
0	X	0	X	0	X	1
0	X	0	X	X	0	1
0	X	X	0	0	X	1
0	X	X	0	X	0	1
1	1	X	X	X	X	0
X	0	0	X	0	X	1
X	0	0	X	X	0	1
X	0	X	0	0	X	1
X	0	X	0	X	0	1
X	X	1	1	X	X	0
X	X	X	X	1	1	0

Layout

Files

See also

AOI322 - a 3-2-2-input AND-OR-Invert gate
AOI332 - a 3-3-2-input AND-OR-Invert gate
AOI333 - a 3-3-3-input AND-OR-Invert gate

Cell

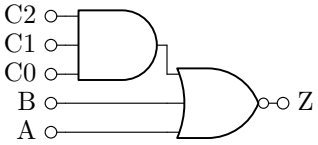
AOI311 - a 3-1-1-input AND-OR-Invert gate

Synopsys

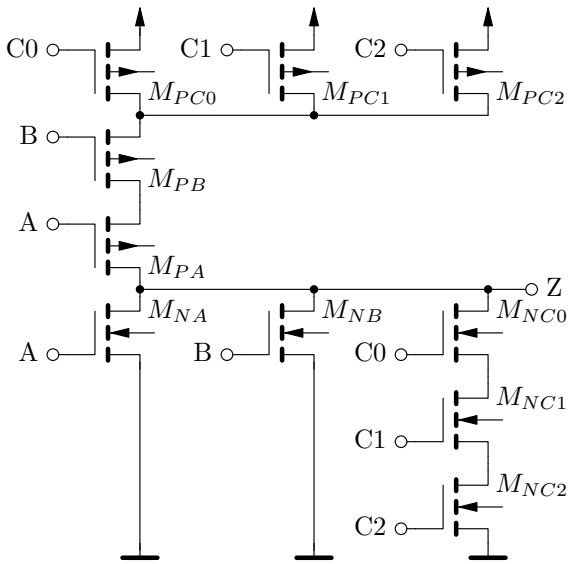
AOI311(Z, C2, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $3T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee B \vee A)$$

C2	C1	C0	B	A	Z
0	X	X	0	0	1
1	1	1	X	X	0
X	0	X	0	0	1
X	X	0	0	0	1
X	X	X	1	X	0
X	X	X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI211 - a 2-1-1-input AND-OR-Invert gate

Cell

AOI321 - a 3-2-1-input AND-OR-Invert gate

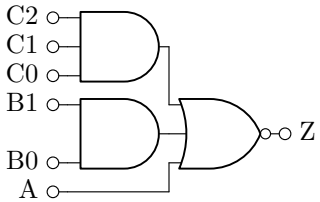
Synopsys

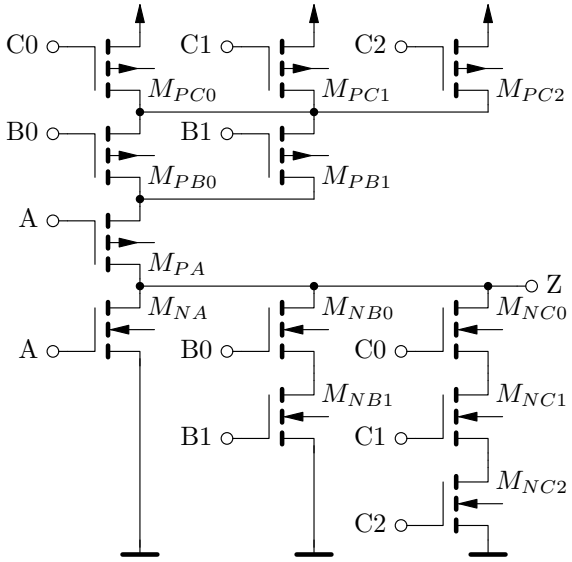
AOI321(Z, C2, C1, C0, B1, B0, A)

Description

Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 12T total)





Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B1 \wedge B0) \vee A)$$

Usage

Fan-in / Fan-out

Layout

Files

See also

AOI311 - a 3-1-1-input AND-OR-Invert gate
AOI331 - a 3-3-1-input AND-OR-Invert gate

Cell

AOI322 - a 3-2-2-input AND-OR-Invert gate

Synopsys

AOI322(Z, C2, C1, C0, B1, B0, A1, A0)

Description

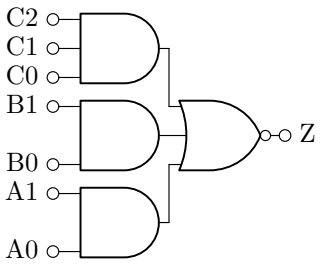
Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)

Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B1 \wedge B0) \vee (A1 \wedge A0))$$

C2	C1	C0	B1	B0	A	Z
0	X	X	0	X	0	1
0	X	X	X	0	0	1
1	1	1	X	X	X	0
X	0	X	0	X	0	1
X	0	X	X	0	0	1
X	X	0	0	X	0	1
X	X	0	X	0	0	1
X	X	X	1	1	X	0
X	X	X	X	X	1	0



Usage

Fan-in / Fan-out

Layout

Files

See also

AOI222 - a 2-2-2-input AND-OR-Invert gate
AOI332 - a 3-2-2-input AND-OR-Invert gate
AOI333 - a 3-3-3-input AND-OR-Invert gate

Cell

AOI331 - a 3-3-1-input AND-OR-Invert gate

Synopsys

AOI331(Z, C2, C1, C0, B2, B1, B0, A)

Description

Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)

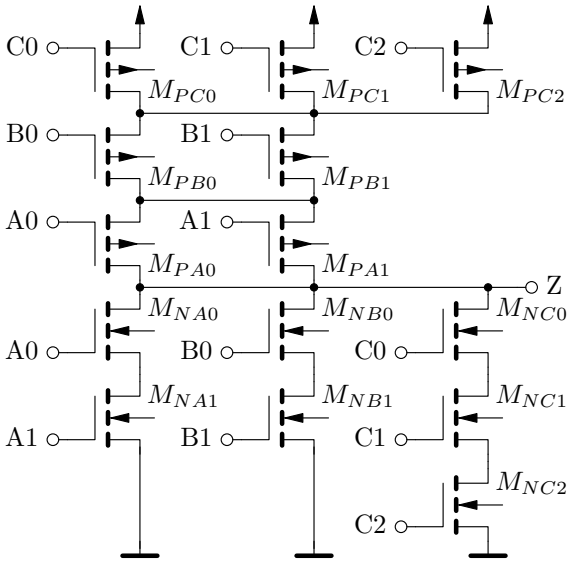
Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee A)$$

Usage

Fan-in / Fan-out

Layout



C2	C1	C0	B1	B0	A1	A0	Z
0	X	X	0	X	0	X	1
0	X	X	0	X	X	0	1
0	X	X	X	0	0	X	1
0	X	X	X	0	X	0	1
1	1	1	X	X	X	X	0
X	0	X	0	X	0	X	1
X	0	X	0	X	X	0	1
X	0	X	X	0	0	X	1
X	0	X	X	0	X	0	1
X	X	0	0	X	0	X	1
X	X	0	0	X	X	0	1
X	X	0	X	0	0	X	1
X	X	0	X	0	X	0	1
X	X	X	1	1	X	X	0
X	X	X	X	X	1	1	0

Files

See also

AOI221 - a 2-2-1-input AND-OR-Invert gate
AOI321 - a 3-2-1-input AND-OR-Invert gate

Cell

AOI332 - a 3-3-2-input AND-OR-Invert gate

Synopsys

AOI332(Z, C2, C1, C0, B2, B1, B0, A1, A0)

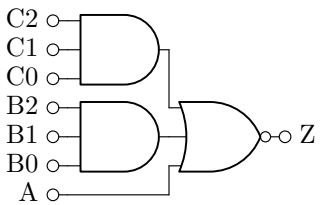
Description

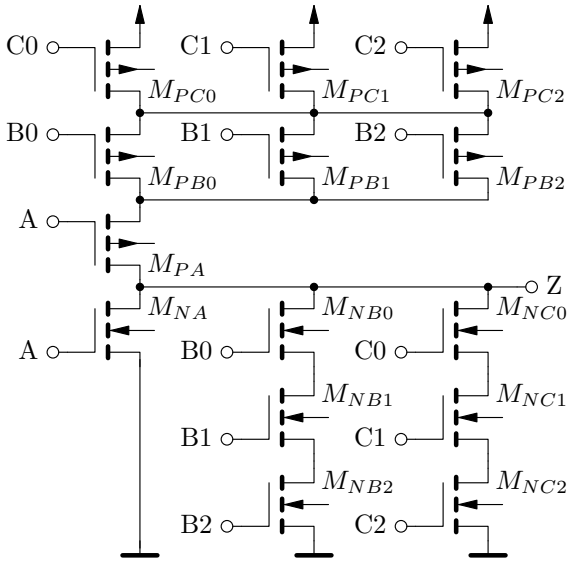
Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 16T total)

Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee (A1 \wedge A0))$$





Usage

Fan-in / Fan-out

Layout

Files

See also

AOI222 - a 2-2-2-input AND-OR-Invert gate
AOI322 - a 3-2-2-input AND-OR-Invert gate
AOI333 - a 3-3-3-input AND-OR-Invert gate

Cell

AOI333 - a 3-3-3-input AND-OR-Invert gate

Synopsys

AOI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0)

Description

Circuit

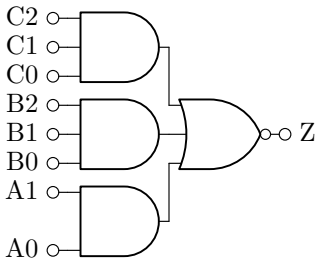
Schematic (one stage, $3T_p/3T_n$ stacked, 18T total)

Truth Table

$$Z = \neg((C2 \wedge C1 \wedge C0) \vee (B2 \wedge B1 \wedge B0) \vee (A2 \wedge A1 \wedge A0))$$

Usage

C2	C1	C0	B2	B1	B0	A	Z
0	X	X	0	X	X	0	1
0	X	X	X	0	X	0	1
0	X	X	X	X	0	0	1
1	1	1	X	X	X	X	0
X	0	X	0	X	X	0	1
X	0	X	X	0	X	0	1
X	0	X	X	X	0	0	1
X	X	0	0	X	X	0	1
X	X	0	X	0	X	0	1
X	X	0	X	X	0	0	1
X	X	X	1	1	1	X	0
X	X	X	X	X	X	1	0



Fan-in / Fan-out

Layout

Files

See also

AOI222 - a 2-2-2-input AND-OR-Invert gate
AOI322 - a 3-2-2-input AND-OR-Invert gate
AOI332 - a 3-3-2-input AND-OR-Invert gate

Cell

BUF - a Buffer gate

Synopsys

BUF(Z, A)

Description

Circuit

Schematic (two stages, $1T_p/1T_n$ stacked, 4T total)

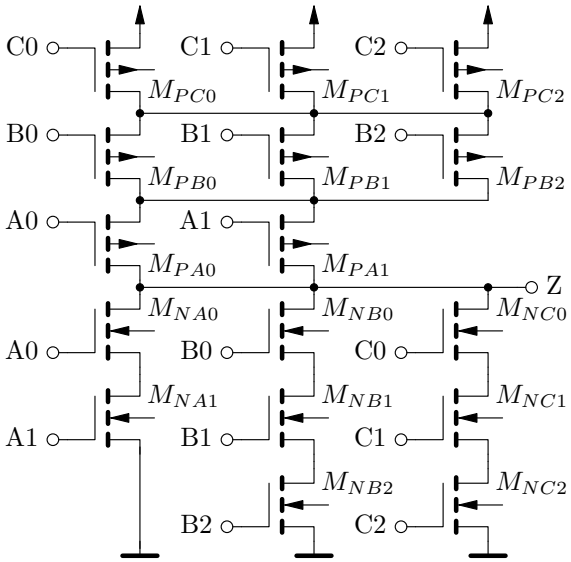
Truth Table

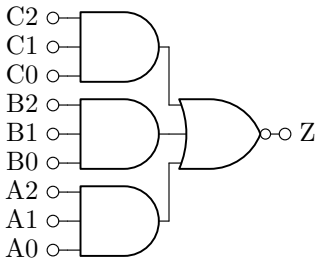
$$Z = A$$

Usage

Fan-in / Fan-out

Layout





Files

See also

INV - a Not (or Inverter) gate

Cell

EQ2 - a 2-input Equality (or XNOR) gate

Synopsys

EQ2(Z, B, A)

Description

Circuit

Schematic (two stages, $2T_p/2T_n$ stacked, 10T total)

Truth Table

$$Z = \neg(B \oplus A)$$

Usage

Fan-in / Fan-out

Keep attention - Fan-in is doubled

Layout

C2	C1	C0	B2	B1	B0	A1	A0	Z
0	X	X	0	X	X	0	X	1
0	X	X	0	X	X	X	0	1
0	X	X	X	0	X	0	X	1
0	X	X	X	0	X	X	0	1
0	X	X	X	X	0	0	X	1
0	X	X	X	X	0	X	0	1
1	1	1	X	X	X	X	X	0
X	0	X	0	X	X	0	X	1
X	0	X	0	X	X	X	0	1
X	0	X	X	0	X	0	X	1
X	0	X	X	0	X	X	0	1
X	0	X	X	X	0	0	X	1
X	0	X	X	X	0	X	0	1
X	X	0	0	X	X	0	X	1
X	X	0	0	X	X	X	0	1
X	X	0	X	0	X	0	X	1
X	X	0	X	0	X	X	0	1
X	X	0	X	X	0	0	X	1
X	X	0	X	X	0	X	0	1
X	X	X	1	1	1	X	X	0
X	X	X	X	X	X	1	1	0

Files

Simulation

☐ `./Sources/verilog/EQ2.v` - Verilog-95 Cell Model

☐ `./Sources/verilog/EQ2_switch.v` - Verilog-2001 Switch-Level Model

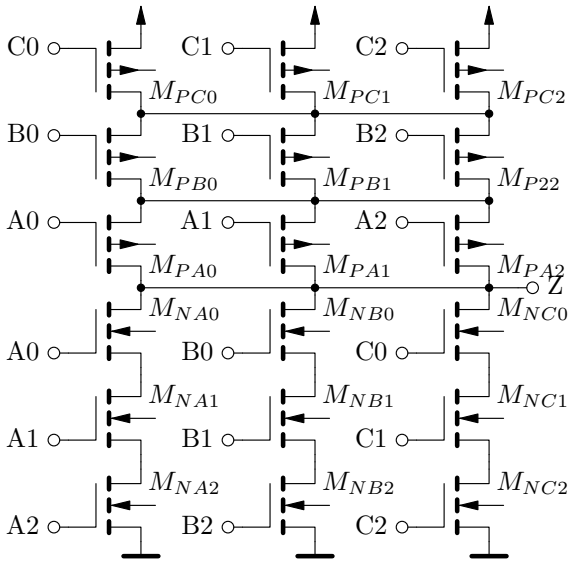
☐ `./TBench/verilog/tb_EQ2.v` - Verilog-2001 Self-checking Testbench

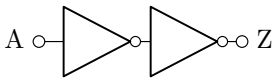
Physical Layout

✓ ?

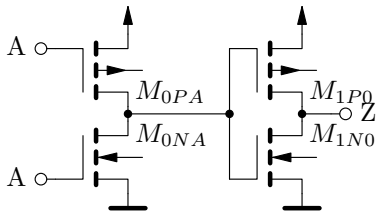
See also

XOR2 - a 2-input Exclusive-OR (or XOR) gate

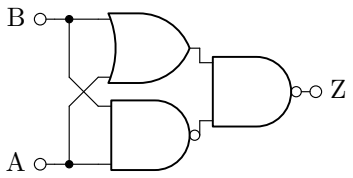


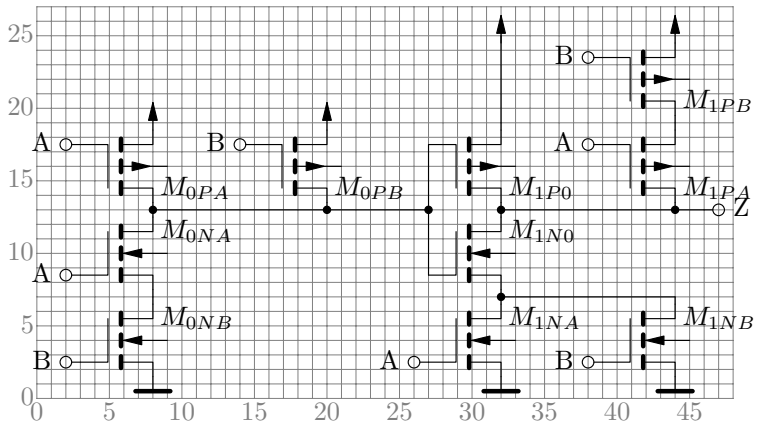


C2	C1	C0	B2	B1	B0	A2	A1	A0	Z
0	X	X	0	X	X	0	X	X	1
0	X	X	0	X	X	X	0	X	1
0	X	X	0	X	X	X	X	0	1
0	X	X	X	0	X	0	X	X	1
0	X	X	X	0	X	X	0	X	1
0	X	X	X	0	X	X	X	0	1
0	X	X	X	X	0	0	X	X	1
0	X	X	X	X	0	X	0	X	1
0	X	X	X	X	0	X	X	0	1
1	1	1	X	X	X	X	X	X	0
X	0	X	0	X	X	0	X	X	1
X	0	X	0	X	X	X	0	X	1
X	0	X	0	X	X	X	X	0	1
X	0	X	X	0	X	0	X	X	1
X	0	X	X	0	X	X	0	X	1
X	0	X	X	0	X	X	X	0	1
X	0	X	X	X	0	0	X	X	1
X	0	X	X	X	0	X	0	X	1
X	0	X	X	X	0	X	X	0	1
X	X	0	0	X	X	0	X	X	1
X	X	0	0	X	X	X	0	X	1
X	X	0	0	X	X	X	X	0	1
X	X	0	X	0	X	0	X	X	1
X	X	0	X	0	X	X	0	X	1
X	X	0	X	0	X	X	X	0	1
X	X	0	X	X	0	0	X	X	1
X	X	0	X	X	0	X	0	X	1
X	X	0	X	X	0	X	X	0	1
X	X	X	1	1	1	X	X	X	0
X	X	X	X	X	X	1	1	1	0



A	Z
0	0
1	1





B	A	Z
0	0	1
0	1	0
1	0	0
1	1	1

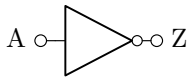
2.4 INV - a Not (or Inverter) gate

Synopsys

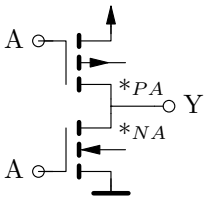
INV (Y A)

Description

Circuit



Schematic (one stage, $1T_p/1T_n$ stacked, $2T$ total)



Truth Table

$Z = \neg A$

A	Z
0	1
1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

BUF - a Buffer gate

Cell

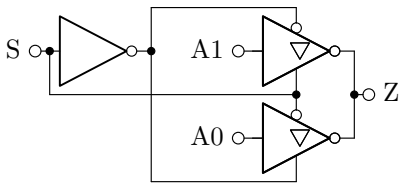
MUXI2 - a 2-to-1 Multiplexor Invert cell

Synopsys

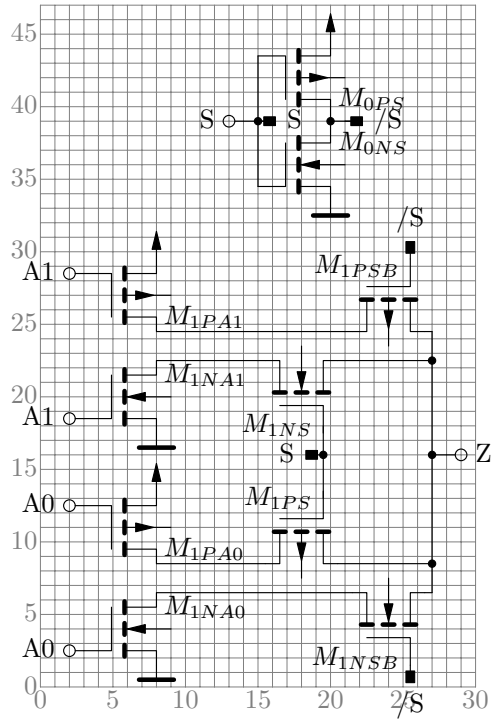
MUXI2(Z, S, A1, A0)

Description

Circuit



Schematic (two stages, $2T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = \neg(A1 \wedge S) \vee \neg(A0 \wedge \neg S))$$

S	A1	A0	Z
0	X	0	1
0	X	1	0
1	0	X	1
1	1	X	0

Usage

Fan-in / Fan-out

Layout

Files

See also

MUXI3 - a 3-to-1 Multiplexor Invert cell
MUXI4 - a 4-to-1 Multiplexor Invert cell

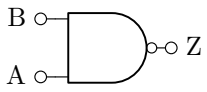
2.5 NAND2 - a 2-input Not-AND (or NAND) gate

Synopsys

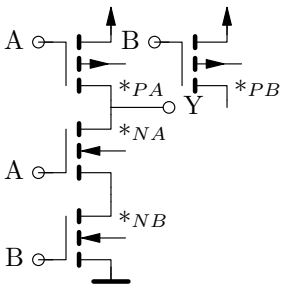
NAND2 (Y B A)

Description

Circuit



Schematic (one stage, $1T_p/2T_n$ stacked, $4T$ total)



Truth Table

$$Z = \neg(B \wedge A)$$

B	A	Z
0	X	1
1	1	0
X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

NAND3 - a 3-input Not-AND (or NAND) gate

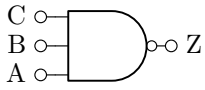
2.6 NAND3 - a 3-input Not-AND (or NAND) gate

Synopsys

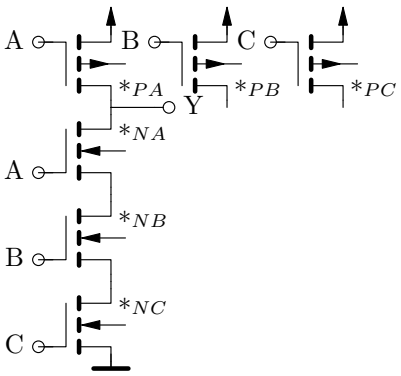
NAND3 (Y C B A)

Description

Circuit



Schematic (one stage, $1T_p/3T_n$ stacked, $6T$ total)



Truth Table

$$Z = \neg(C \wedge B \wedge A)$$

C	B	A	Z
0	X	X	1
1	1	1	0
X	0	X	1
X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

NAND2 - a 2-input Not-AND (or NAND) gate

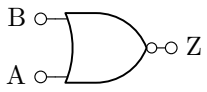
2.7 NOR2 - a 2-input Not-OR (or NOR) gate

Synopsys

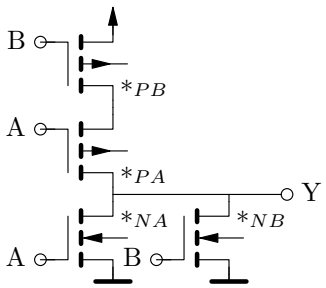
NOR2 (Y B A)

Description

Circuit



Schematic (one stage, $2T_p/1T_n$ stacked, $4T$ total)



Truth Table

$$Z = \neg(B \vee A)$$

B	A	Z
0	0	1
1	X	0
X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

NOR3 - a 3-input Not-OR (or NOR) gate

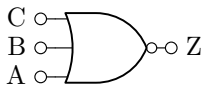
2.8 NOR3 - a 3-input Not-OR (or NOR) gate

Synopsys

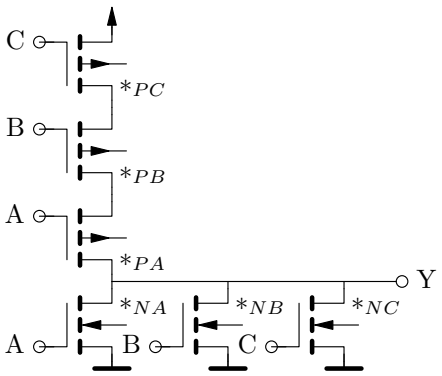
NOR3 (Y C B A)

Description

Circuit



Schematic (one stage, $3T_p/1T_n$ stacked, $6T$ total)



Truth Table

$$Z = \neg(C \vee B \vee A)$$

C	B	A	Z
0	0	0	1
1	X	X	0
X	1	X	0
X	X	1	0

Usage

Fan-in / Fan-out

Layout

Files

See also

NOR2 - a 2-input Not-OR (or NOR) gate

Cell

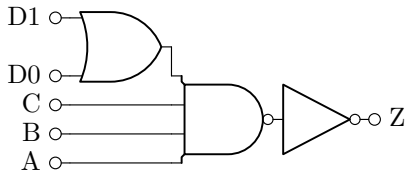
OA2111 - a 2-1-1-1-input OR-AND gate

Synopsys

OA2111(Z, D1, D0, C, B, A)

Description

Circuit



Truth Table

$$Z = (D1 \vee D0) \wedge C \wedge B \wedge A$$

D1	D0	C	B	A	Z
0	0	X	X	X	0
1	X	1	1	1	1
X	1	1	1	1	1
X	X	0	X	X	0
X	X	X	0	X	0
X	X	X	X	0	0

Usage

Fan-in / Fan-out

Layout

Files

See also

OA3111 - a 3-1-1-1-input AND-OR gate

Cell

OA3111 - a 3-1-1-1-input OR-AND gate

Synopsys

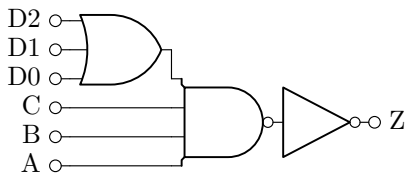
OA3111(Z, D2, D1, D0, C, B, A)

Description

Circuit

Truth Table

$$Z = (D2 \vee D1 \vee D0) \wedge C \wedge B \wedge A$$



D2	D1	D0	C	B	A	Z
0	0	0	X	X	X	0
1	X	X	1	1	1	1
X	1	X	1	1	1	1
X	X	1	1	1	1	1
X	X	X	0	X	X	0
X	X	X	X	0	X	0
X	X	X	X	X	0	0

Usage

Fan-in / Fan-out

Layout

Files

See also

OA2111 - a 2-1-1-1-input AND-OR gate

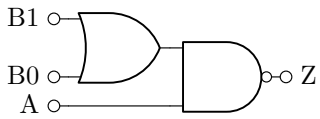
2.9 OAI21 - a 2-1-input OR-AND-Invert gate

Synopsys

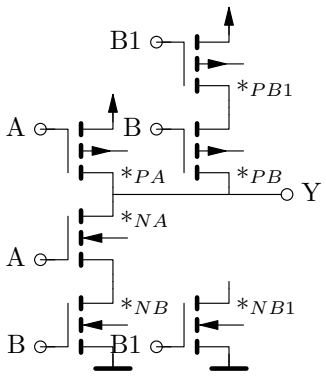
OAI21 (Y B1 B A)

Description

Circuit



Schematic (one stage, $2T_p/2T_n$ stacked, $6T$ total)



Truth Table

$$Z = \neg((B1 \vee B0) \wedge A)$$

B1	B0	A	Z
0	0	X	1
1	X	1	0
X	1	1	0
X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI31 - a 3-1-input OR-AND-Invert gate

Cell

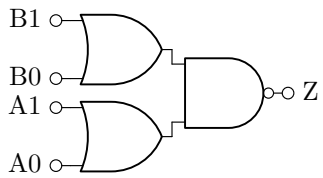
OAI22 - a 2-2-input OR-AND-Invert gate

Synopsys

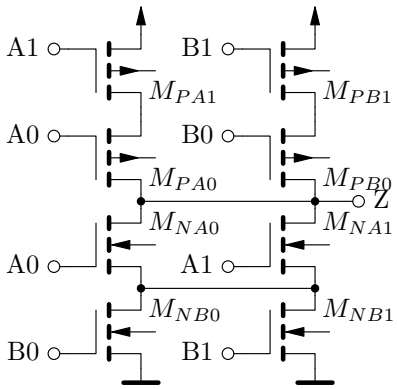
OAI22(Z, B1, B0, A1, A0)

Description

Circuit



Schematic (one stage, $2T_p/2T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((B1 \vee B0) \wedge (A1 \vee A0))$$

B1	B0	A1	A0	Z
0	0	X	X	1
1	X	1	X	0
1	X	X	1	0
X	1	1	X	0
X	1	X	1	0
X	X	0	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI32 - a 3-2-input OR-AND-Invert gate
OAI33 - a 3-3-input OR-AND-Invert gate

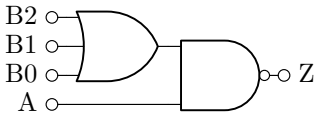
2.10 OAI31 - a 3-1-input OR-AND-Invert gate

Synopsys

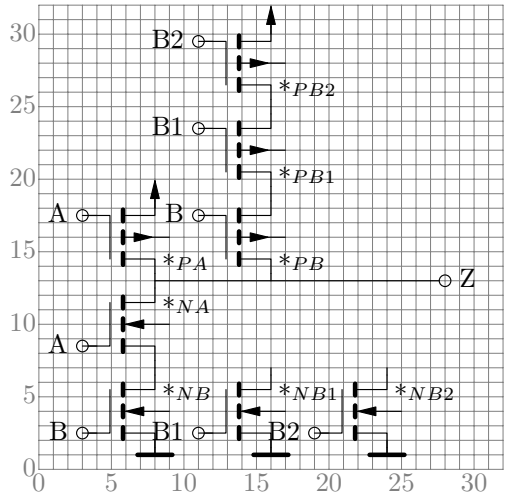
OAI31 (Y B2 B1 B A)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, $8T$ total)



Truth Table

$$Z = \neg((B2 \vee B1 \vee B0) \wedge A)$$

B2	B1	B0	A	Z
0	0	0	X	1
1	X	X	1	0
X	1	X	1	0
X	X	1	1	0
X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI21 - a 2-1-input OR-AND-Invert gate

Cell

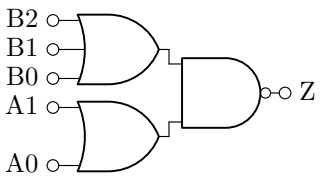
OAI32 - a 3-2-input OR-AND-Invert gate

Synopsys

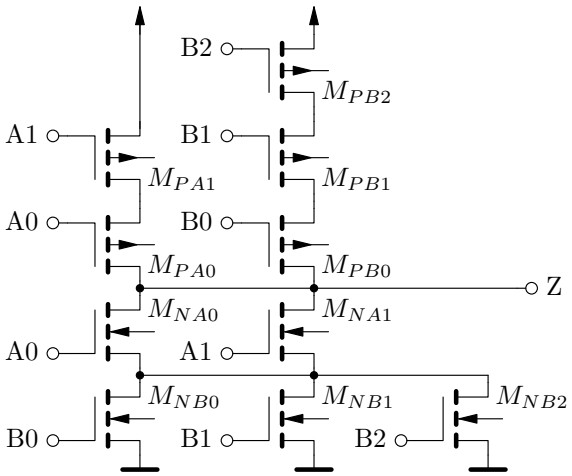
OAI32(Z, B2, B1, B0, A1, A0)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((B2 \vee B1 \vee B0) \wedge (A1 \vee A0))$$

B2	B1	B0	A1	A0	Z
0	0	0	X	X	1
1	X	X	1	X	0
1	X	X	X	1	0
X	1	X	1	X	0
X	1	X	X	1	0
X	X	1	1	X	0
X	X	1	X	1	0
X	X	X	0	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI22 - a 2-2-input OR-AND-Invert gate
OAI33 - a 3-3-input OR-AND-Invert gate

Cell

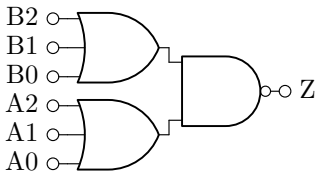
OAI33 - a 3-3-input OR-AND-Invert gate

Synopsys

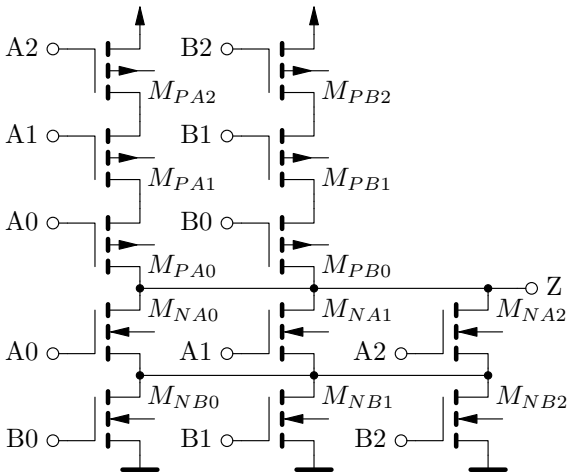
OAI33(Z, B2, B1, B0, A2, A1, A0)

Description

Circuit



Schematic (one stage, $3T_p/2T_n$ stacked, 12T total)



Truth Table

$$Z = \neg((B2 \vee B1 \vee B0) \wedge (A2 \vee A1 \vee A0))$$

Usage

Fan-in / Fan-out

Layout

Files

B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	1
1	X	X	1	X	X	0
1	X	X	X	1	X	0
1	X	X	X	X	1	0
X	1	X	1	X	X	0
X	1	X	X	1	X	0
X	1	X	X	X	1	0
X	X	1	1	X	X	0
X	X	1	X	1	X	0
X	X	1	X	X	1	0
X	X	X	0	0	0	1

See also

OAI22 - a 2-2-input OR-AND-Invert gate
OAI32 - a 3-2-input OR-AND-Invert gate

Cell

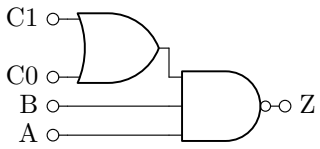
OAI211 - a 2-1-1-input OR-AND-Invert gate

Synopsys

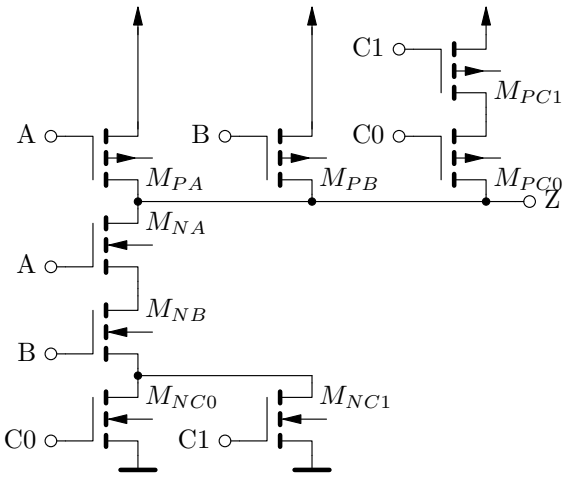
OAI211(Z, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 8T total)



Truth Table

$$Z = \neg((C1 \vee C0) \wedge B \wedge A)$$

C1	C0	B	A	Z
0	0	X	X	1
1	X	1	1	0
X	1	1	1	0
X	X	0	X	1
X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI311 - a 3-1-1-input OR-AND-Invert gate

Cell

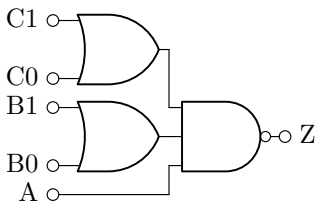
OAI221 - a 2-2-1-input OR-AND-Invert gate

Synopsys

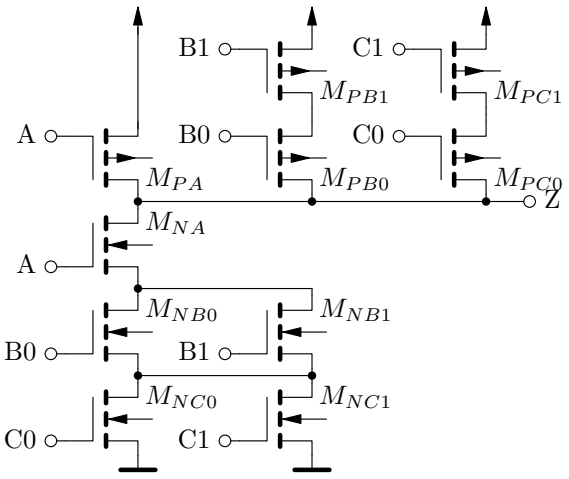
OAI221(Z, C1, C0, B1, B0, A)

Description

Circuit



Schematic (one stage, $2T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C1 \vee C0) \wedge (B1 \vee B0) \wedge A)$$

C1	C0	B1	B0	A	Z
0	0	X	X	X	1
1	X	1	X	1	0
1	X	X	1	1	0
X	1	1	X	1	0
X	1	X	1	1	0
X	X	0	0	X	1
X	X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI321 - a 3-2-1-input OR-AND-Invert gate
OAI331 - a 3-3-1-input OR-AND-Invert gate

Cell

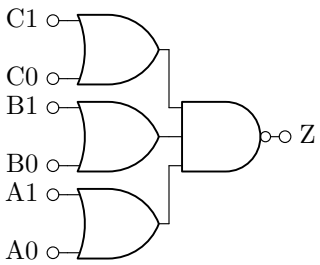
OAI222 - a 2-2-2-input OR-AND-Invert gate

Synopsys

OAI222(Z, C1, C0, B1, B0, A1, A0)

Description

Circuit



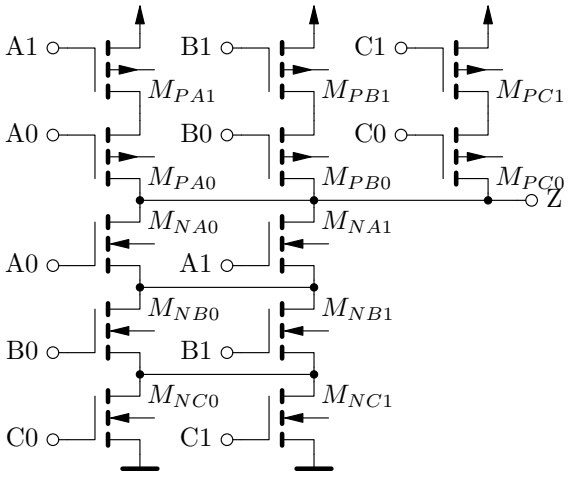
Schematic (one stage, $2T_p/3T_n$ stacked, 12T total)

Truth Table

$$Z = \neg((C1 \vee C0) \wedge (B1 \vee B0) \wedge (A1 \vee A0))$$

Usage

Fan-in / Fan-out



C1	C0	B1	B0	A1	A0	Z
0	0	X	X	X	X	1
1	X	1	X	1	X	0
1	X	1	X	X	1	0
1	X	X	1	1	X	0
1	X	X	1	X	1	0
X	1	1	X	1	X	0
X	1	1	X	X	1	0
X	1	X	1	1	X	0
X	1	X	1	X	1	0
X	X	0	0	X	X	1
X	X	X	X	0	0	1

Layout

Files

See also

OAI322 - a 2-2-2-input OR-AND-Invert gate
OAI332 - a 3-3-2-input OR-AND-Invert gate
OAI333 - a 3-3-3-input OR-AND-Invert gate

Cell

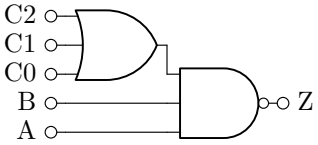
OAI311 - a 3-1-1-input OR-AND-Invert gate

Synopsys

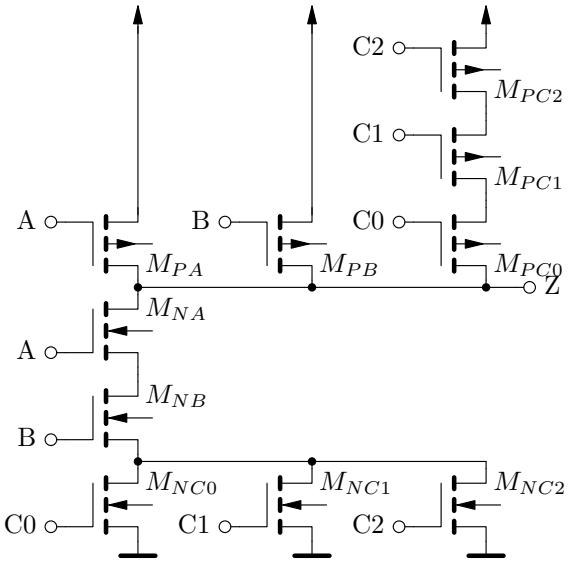
OAI311(Z, C2, C1, C0, B, A)

Description

Circuit



Schematic (one stage, $3T_p/3T_n$ stacked, 10T total)



Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge B \wedge A)$$

C2	C1	C0	B	A	Z
0	0	0	X	X	1
1	X	X	1	1	0
X	1	X	1	1	0
X	X	1	1	1	0
X	X	X	0	X	1
X	X	X	X	0	1

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI211 - a 2-1-1-input OR-AND-Invert gate

Cell

OAI321 - a 3-2-1-input OR-AND-Invert gate

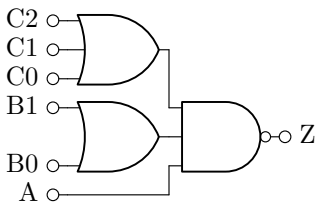
Synopsys

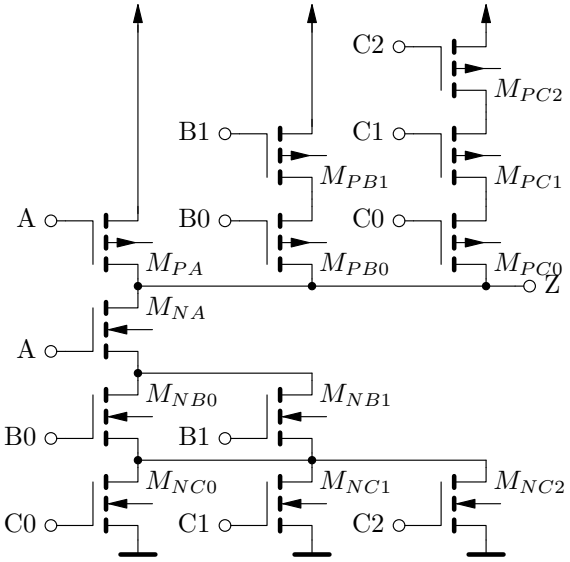
OAI321(Z, C2, C1, C0, B1, B0, A)

Description

Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 12T total)





Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B1 \vee B0) \wedge A)$$

Usage

Fan-in / Fan-out

Layout

Files

See also

OAI221 - a 2-2-1-input OR-AND-Invert gate
OAI331 - a 3-3-1-input OR-AND-Invert gate

Cell

OAI322 - a 3-2-2-input OR-AND-Invert gate

Synopsys

OAI322(Z, C2, C1, C0, B1, B0, A1, A0)

Description

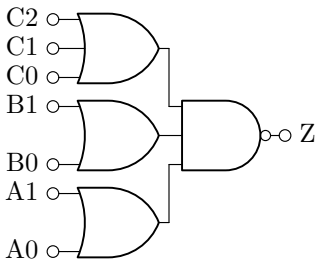
Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)

Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B1 \vee B0) \wedge (A1 \vee A0))$$

C2	C1	C0	B1	B0	A	Z
0	0	0	X	X	X	1
1	X	X	1	X	1	0
1	X	X	X	1	1	0
X	1	X	1	X	1	0
X	1	X	X	1	1	0
X	X	1	1	X	1	0
X	X	1	X	1	1	0
X	X	X	0	0	X	1
X	X	X	X	X	0	1



Usage

Fan-in / Fan-out

Layout

Files

See also

OAI222 - a 2-2-2-input OR-AND-Invert gate
OAI332 - a 3-3-2-input OR-AND-Invert gate
OAI333 - a 3-3-3-input OR-AND-Invert gate

Cell

OAI331 - a 3-3-1-input OR-AND-Invert gate

Synopsys

OAI331(Z, C2, C1, C0, B2, B1, B0, A)

Description

Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)

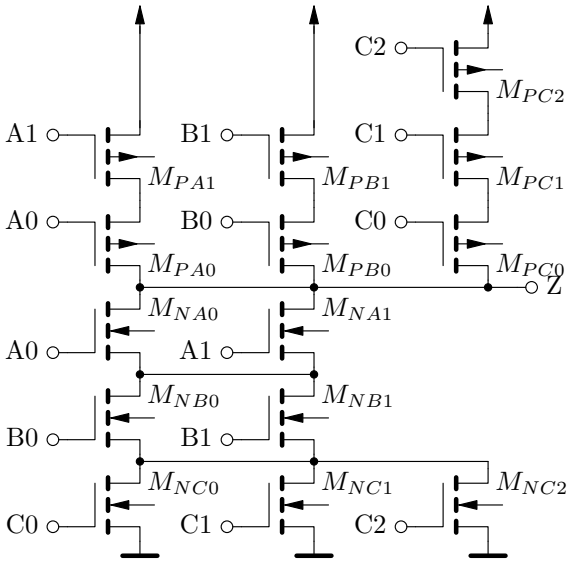
Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B2 \vee B1 \vee B0) \wedge A)$$

Usage

Fan-in / Fan-out

Layout



C2	C1	C0	B1	B0	A1	A0	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	1	X	0
1	X	X	1	X	X	1	0
1	X	X	X	1	1	X	0
1	X	X	X	1	X	1	0
X	1	X	1	X	1	X	0
X	1	X	1	X	X	1	0
X	1	X	X	1	1	X	0
X	1	X	X	1	X	1	0
X	X	1	1	X	1	X	0
X	X	1	1	X	X	1	0
X	X	1	X	1	1	X	0
X	X	1	X	1	X	1	0
X	X	X	0	0	X	X	1
X	X	X	X	X	0	0	1

Files

See also

OAI221 - a 2-2-1-input OR-AND-Invert gate
OAI321 - a 3-2-1-input OR-AND-Invert gate

Cell

OAI332 - a 3-3-2-input OR-AND-Invert gate

Synopsys

OAI332(Z, C2, C1, C0, B2, B1, B0, A1, A0)

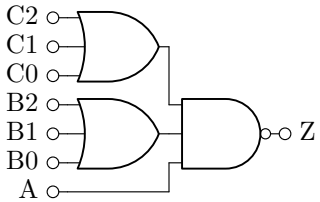
Description

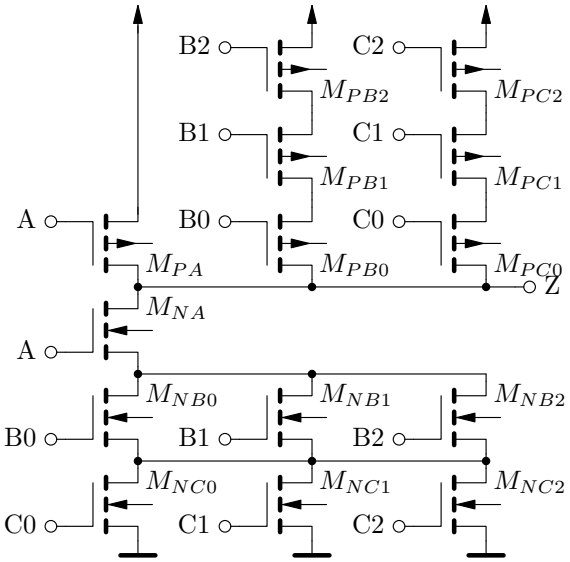
Circuit

Schematic (one stage, $3T_p/3T_n$ stacked, 14T total)

Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B1 \vee B0) \wedge (A1 \vee A0))$$





Usage

Fan-in / Fan-out

Layout

Files

See also

OAI222 - a 2-2-2-input OR-AND-Invert gate
OAI322 - a 3-2-2-input OR-AND-Invert gate
OAI333 - a 3-3-3-input OR-AND-Invert gate

Cell

OAI333 - a 3-3-3-input OR-AND-Invert gate

Synopsys

OAI333(Z, C2, C1, C0, B2, B1, B0, A2, A1, A0)

Description

Circuit

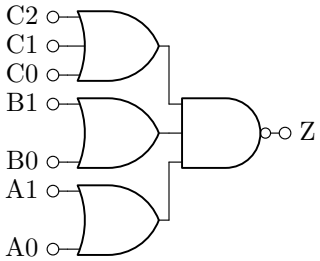
Schematic (one stage, $3T_p/3T_n$ stacked, 18T total)

Truth Table

$$Z = \neg((C2 \vee C1 \vee C0) \wedge (B2 \vee B1 \vee B0) \wedge (A2 \vee A1 \vee A0))$$

Usage

C2	C1	C0	B2	B1	B0	A	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	X	1	0
1	X	X	X	1	X	1	0
1	X	X	X	X	1	1	0
X	1	X	1	X	X	1	0
X	1	X	X	1	X	1	0
X	1	X	X	X	1	1	0
X	X	1	1	X	X	1	0
X	X	1	X	1	X	1	0
X	X	1	X	X	1	1	0
X	X	X	0	0	0	X	1
X	X	X	X	X	X	0	1



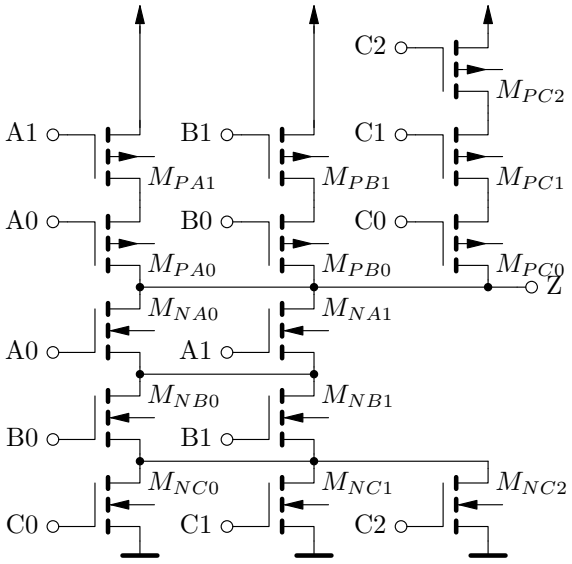
Fan-in / Fan-out

Layout

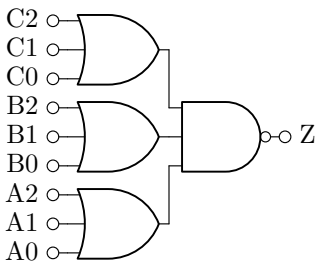
Files

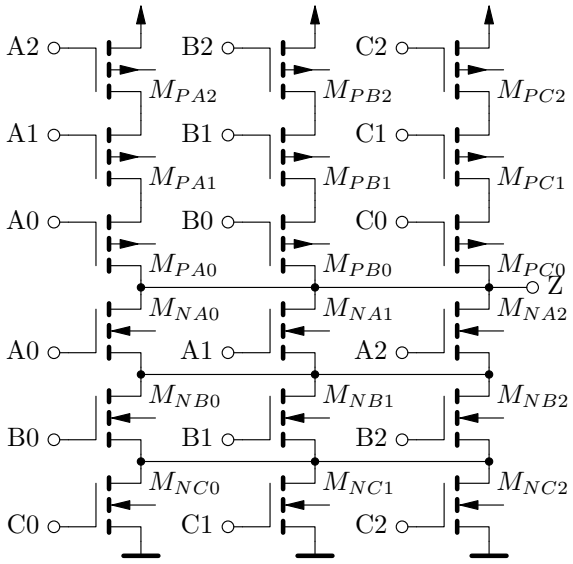
See also

OAI222 - a 2-2-2-input OR-AND-Invert gate
OAI322 - a 3-2-2-input OR-AND-Invert gate
OAI332 - a 3-3-2-input OR-AND-Invert gate



C2	C1	C0	B1	B0	A1	A0	Z
0	0	0	X	X	X	X	1
1	X	X	1	X	1	X	0
1	X	X	1	X	X	1	0
1	X	X	X	1	1	X	0
1	X	X	X	1	X	1	0
X	1	X	1	X	1	X	0
X	1	X	1	X	X	1	0
X	1	X	X	1	1	X	0
X	1	X	X	1	X	1	0
X	X	1	1	X	1	X	0
X	X	1	1	X	X	1	0
X	X	1	X	1	1	X	0
X	X	1	X	1	X	1	0
X	X	X	0	0	X	X	1
X	X	X	X	X	0	0	1





C2	C1	C0	B2	B1	B0	A2	A1	A0	Z
0	0	0	X	X	X	X	X	X	1
1	X	X	1	X	X	1	X	X	0
1	X	X	1	X	X	X	1	X	0
1	X	X	1	X	X	X	X	1	0
1	X	X	X	1	X	1	X	X	0
1	X	X	X	1	X	X	1	X	0
1	X	X	X	1	X	X	X	1	0
1	X	X	X	X	1	1	X	X	0
1	X	X	X	X	1	X	1	X	0
1	X	X	X	X	1	X	X	1	0
X	1	X	1	X	X	1	X	X	0
X	1	X	1	X	X	X	1	X	0
X	1	X	1	X	X	X	X	1	0
X	1	X	X	1	X	1	X	X	0
X	1	X	X	1	X	X	1	X	0
X	1	X	X	1	X	X	X	1	0
X	1	X	X	X	1	1	X	X	0
X	1	X	X	X	1	X	1	X	0
X	1	X	X	X	1	X	X	1	0
X	X	1	1	X	X	X	1	X	0
X	X	1	1	X	X	X	X	1	0
X	X	1	X	1	X	1	X	X	0
X	X	1	X	1	X	X	1	X	0
X	X	1	X	1	X	X	X	1	0
X	X	1	X	X	1	1	X	X	0
X	X	1	X	X	1	X	1	X	0
X	X	1	X	X	1	X	X	1	0
X	X	X	0	0	0	X	X	X	1
X	X	X	X	X	X	0	0	0	1

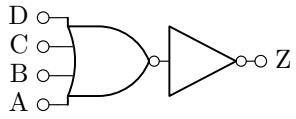
2.11 OR4 - a 4-input OR gate

Synopsys

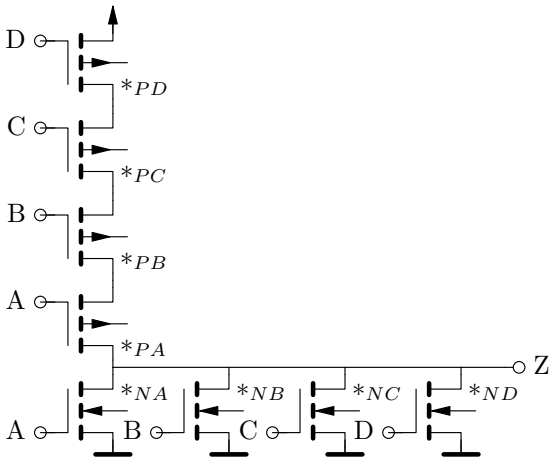
OR4 (Z Y Y D C B A)

Description

Circuit



Schematic (one stage, $4T_p/1T_n$ stacked, $10T$ total)



Truth Table

$$Z = D \vee C \vee B \vee A$$

D	C	B	A	Z
0	0	0	0	0
1	X	X	X	1
X	1	X	X	1
X	X	1	X	1
X	X	X	1	1

Usage

Fan-in / Fan-out

Layout

Files

See also

NOR3 - a 3-input Not-OR (or NOR) gate

Cell

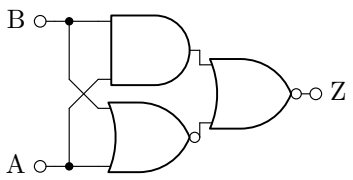
XOR2 - a 2-input Exclusive-OR (or XOR) gate

Synopsys

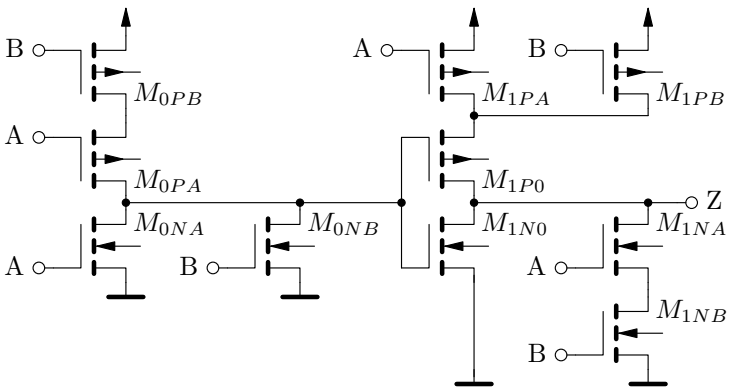
XOR2(Z, B, A)

Description

Circuit



Schematic (two stages, $2T_p/2T_n$ stacked, 10T total)



Truth Table

$$Z = B \oplus A$$

B	A	Z
0	0	0
0	1	1
1	0	1
1	1	0

Usage

Fan-in / Fan-out

Keep attention - Fan-in is doubled

Layout

Files

Simulation

☐ `./Sources/verilog/XOR2.v` - Verilog-95 Cell Model

☐ `./Sources/verilog/XOR2_switch.v` - Verilog-2001 Switch-Level Model

☐ `./TBench/verilog/tb_XOR2.v` - Verilog-2001 Self-checking Testbench

Physical Layout

✓ ?

See also

EQ2 - a 2-input Equality (or XNOR) gate

3 Physical Cells

Cell

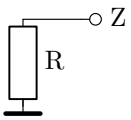
TIE0 - a Tie-low (or pull-down) cell

Synopsys

TIE0(Z)

Description

Circuit



Truth Table

$Z = 0$

Z
0

Usage

Fan-in / Fan-out

Layout

Files

See also

TIE1 - a Tie-high (or pull-up) cell

Cell

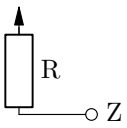
TIE1 - a Tie-high (or pull-up) cell

Synopsys

TIE1(Z)

Description

Circuit



Truth Table

$Z = 1$

Z
1

Usage

Fan-in / Fan-out

Layout

Files

See also

TIE0 - a Tie-low (or pull-down) cell

Cell

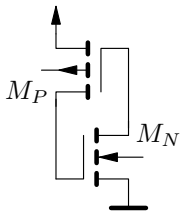
FILL - a Filler cell with capacitance

Synopsys

FILL

Description

Schematic (one stage, 2T total)



Truth Table

No Truth Table applicable.

Usage

Fan-in / Fan-out

Layout

Files

See also VDDIO
GND
ANA