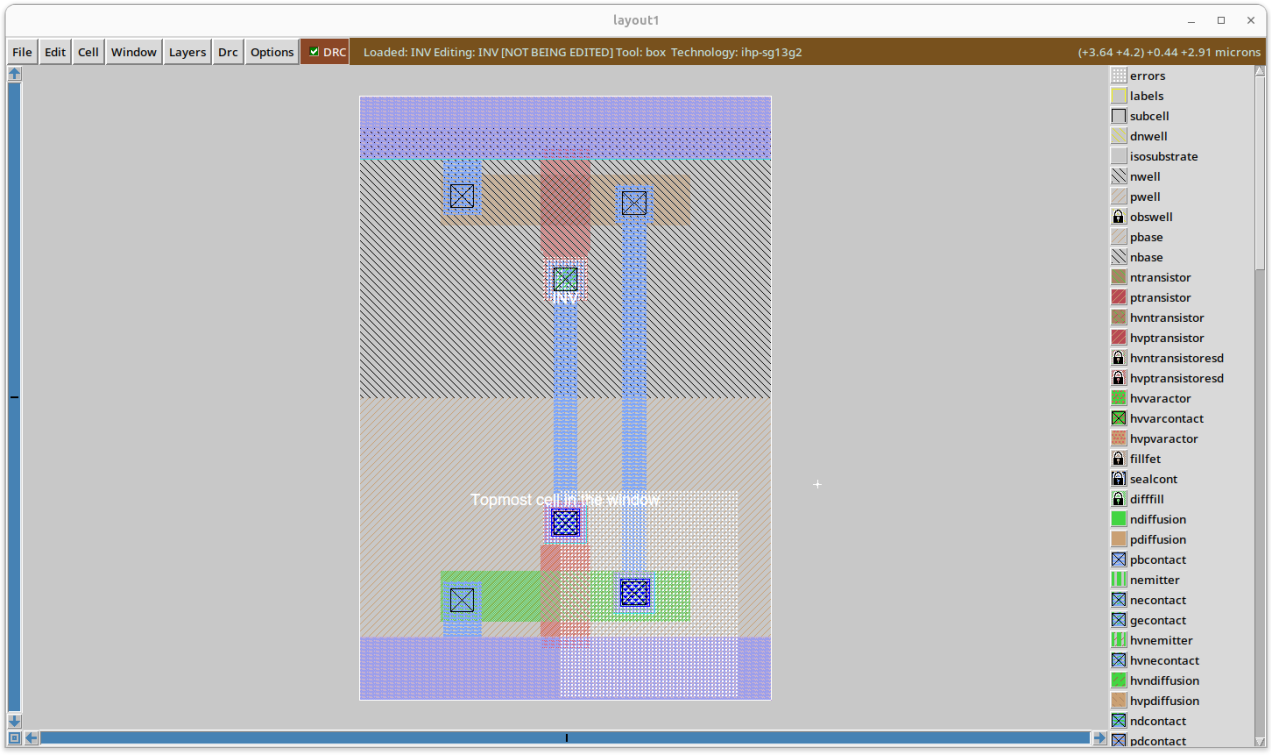
In the last few days I have helped David with the standard cell library generator. At first I have reviewed all the changes David made:

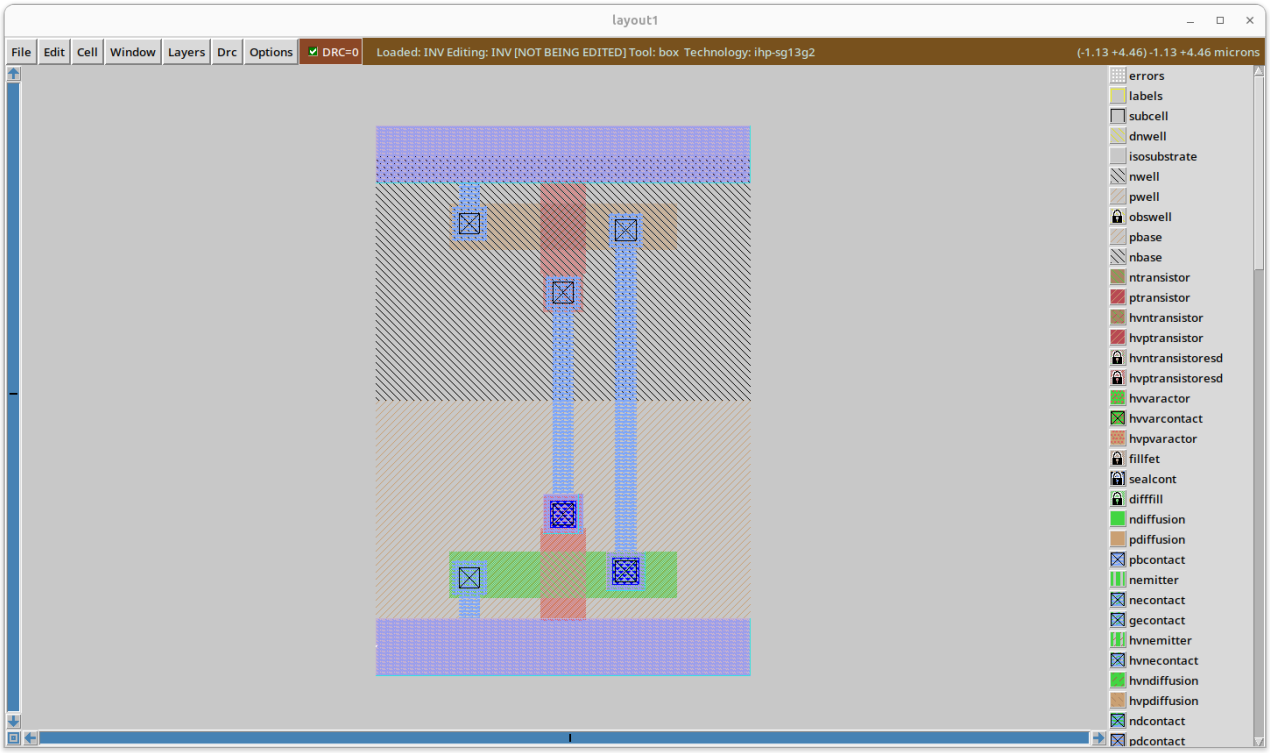
Properly handling magscale now	David Lanzendörfer <leviathan@libr	2025-07-30 01:30:14
Update include path name for file	David Lanzendörfer <leviathan@libr	2025-07-30 01:28:18
Adding magscale info for Skywater	David Lanzendörfer <leviathan@libr	2025-07-30 01:14:03
Updating technology from Volare	David Lanzendörfer <leviathan@libr	2025-07-30 01:13:35
Adding SPICE models for SKY130	David Lanzendörfer <leviathan@libr	2025-07-30 01:12:51
Add SPICE expander	David Lanzendörfer <leviathan@libr	2025-07-30 01:10:56
Moving to generic file name for compatibility	David Lanzendörfer <leviathan@libr	2025-07-27 20:19:58
Hack for making make catalog work	David Lanzendörfer <leviathan@libr	2025-07-27 13:17:49
CI/CD: Artifacts	David Lanzendörfer <leviathan@libr	2025-07-27 13:17:12
Change back some values	David Lanzendörfer <leviathan@libr	2025-07-25 18:46:32
Disable LS1U for now and store logs	David Lanzendörfer <leviathan@libr	2025-07-23 19:01:12
Solve issue with metal1	David Lanzendörfer <leviathan@libr	2025-07-23 18:22:44
Solve issue with metal1	David Lanzendörfer <leviathan@libr	2025-07-23 18:21:44
Update db unit, so that routing doesn't fail	David Lanzendörfer <leviathan@libr	2025-07-23 16:42:34
Set db_unit is 1e-3	David Lanzendörfer <leviathan@libr	2025-07-23 16:20:45
Update technology from LibrePDK	David Lanzendörfer <leviathan@libr	2025-07-23 16:13:18
Remove tab	David Lanzendörfer <leviathan@libr	2025-07-23 16:08:37
Try another approach	David Lanzendörfer <leviathan@libr	2025-07-23 16:06:33
Activate venv	David Lanzendörfer <leviathan@libr	2025-07-23 15:27:12
Maybe this way?	David Lanzendörfer <leviathan@libr	2025-07-23 15:25:14
Again without -l	David Lanzendörfer <leviathan@libr	2025-07-23 15:22:59
different entrypoint?	David Lanzendörfer <leviathan@libr	2025-07-23 15:18:48
Define BASH as entry point in CI/CD definition	David Lanzendörfer <leviathan@libr	2025-07-23 15:13:26
Add more build jobs	David Lanzendörfer <leviathan@libr	2025-07-23 14:46:29
Use the correct image	David Lanzendörfer <leviathan@libr	2025-07-23 14:40:00
Update build task	David Lanzendörfer <leviathan@libr	2025-07-23 14:36:48
Test CI job	David Lanzendörfer <leviathan@libr	2025-07-23 10:07:26
Update .gitlab-ci.yml file	David Lanzendörfer <leviathan@libr	2025-07-23 10:03:39
Use correct type for capacity values	David Lanzendörfer <leviathan@libr	2025-07-23 08:36:32
Cleaning up OASIS files	Philipp Gühring <pg@futureware.at	2025-09-16 11:10:05

After the review, I merged the changes:

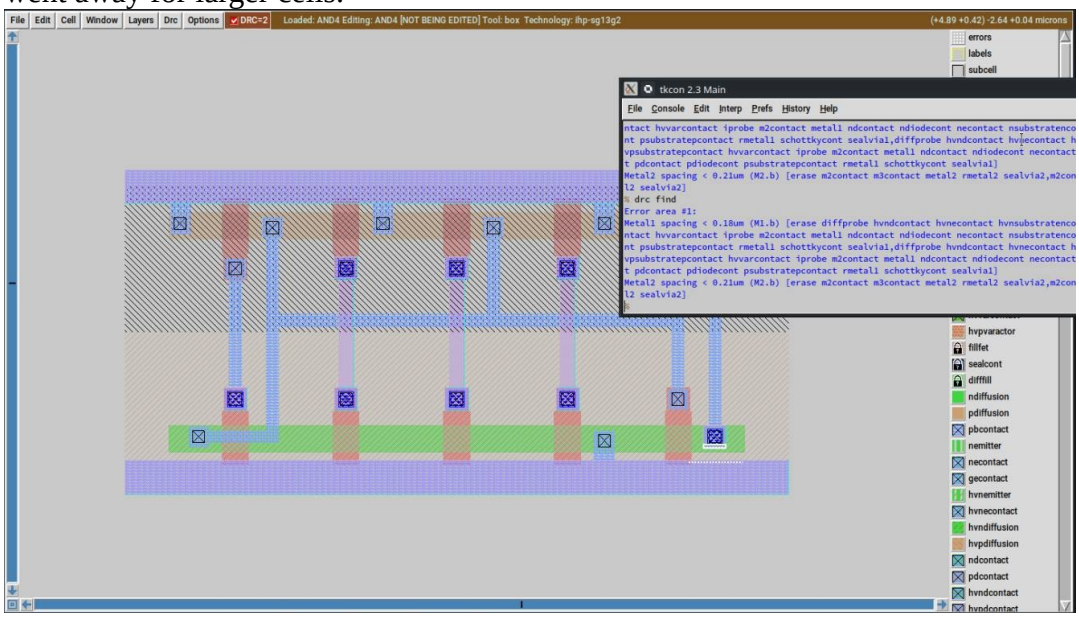
Lokale Änderungen, nicht bereitgestellt		
master remotes/origin/master Adding dlayoutall and clearing	Philipp Gühring <pg@futureware.at>	2025-09-23 15:26:41
Slowing down the updates	Philipp Gühring <pg@futureware.at>	2025-09-23 15:25:49
Merge branch 'master' of https://gitlab.libresilicon.com/generator-toc	Philipp Gühring <pg@futureware.at>	2025-09-23 13:23:48
remotes/lev/master Adding enclosure rule back in	David Lanzendörfer <leviathan@libresilicon.com>	2025-09-22 20:33:09
Switching to IHP SG13G2	Philipp Gühring <pg@futureware.at>	2025-09-23 13:23:14
Adding more cell samples	Philipp Gühring <pg@futureware.at>	2025-09-20 00:31:57
10 more nm to get rid of metal2 violations	Philipp Gühring <pg@futureware.at>	2025-09-20 00:22:45
Adding cell templates	Philipp Gühring <pg@futureware.at>	2025-09-19 23:56:19
Avoiding metal2 DRC errors for bigger cells	Philipp Gühring <pg@futureware.at>	2025-09-18 21:18:05
Fixed a metal2 spacing violation	Philipp Gühring <pg@futureware.at>	2025-09-17 22:36:22
Merge branch 'master' of https://gitlab.libresilicon.com/generator-	Philipp Gühring <pg@futureware.at>	2025-09-17 22:29:26
Adjusting layer name for poly contact	David Lanzendörfer <leviathan@libresilicon.com>	2025-09-17 22:26:17
Correcting and disabling DRC rules	Philipp Gühring <pg@futureware.at>	2025-09-17 22:13:26
Adding LibreCell parameter documentation	Philipp Gühring <pg@futureware.at>	2025-09-17 21:35:12
Making it compatible to sg13g2 cells	Philipp Gühring <pg@futureware.at>	2025-09-17 21:34:35
Correcting many DRC rules, still some TODO	Philipp Gühring <pg@futureware.at>	2025-09-17 01:18:25
Re-Enabled correct scaling	Philipp Gühring <pg@futureware.at>	2025-09-16 21:09:35
Adding dlayout target (docker layout)	Philipp Gühring <pg@futureware.at>	2025-09-16 16:00:13
Merge branch 'master' of https://gitlab.libresilicon.com/generator-	Philipp Gühring <pg@futureware.at>	2025-09-16 11:11:57
Fixing README	David Lanzendörfer <leviathan@libresilicon.com>	2025-09-15 20:51:48
Update README	David Lanzendörfer <leviathan@libresilicon.com>	2025-09-15 18:04:42
Updating some values, trying to fix DRC issues	David Lanzendörfer <leviathan@libresilicon.com>	2025-09-15 16:53:57
IHP: Prepare support for multiple voltages	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-28 21:08:05
Update CI/CD and build targets	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-28 19:15:11
Ignore pycaches	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-28 19:14:49
Remove pyc file	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-28 19:14:11
Fixing design rules	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-28 19:13:05
Load the environment file	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-23 15:03:32
Stage magic layers output	David Lanzendörfer <leviathan@libresilicon.com>	2025-08-22 20:42:04

Then I worked through all the DRC design rules for the IHP SG13G2 library, to make the standard cell layouting working for the IHP process. At first I tested it with a simple inverter cell (INV.cell).



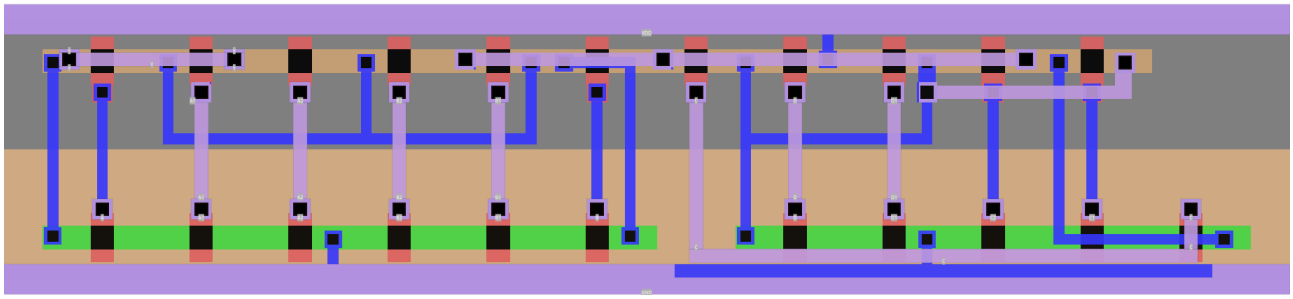


The inverter cell still had some DRC issues, so I reviewed and corrected all the DRC rules and configurations for lclayout. After those were corrected, the INVerter cell was building correctly, no more DRC errors, and this way the cell would be most likely accepted by the factory.
Afterwards I shortly tested a larger AND cell, and discovered that sometimes the vias would be too near to the power rails, so we moved the transistors inwards a few times until all those DRC issues went away for larger cells.



Then we discussed the need for compatibility of our cells with the existing cells supplied by the vendors (like IHP), and we agreed that our cells should be as compatible as feasible, so that they can be mixed&matched with the existing cells. So users of our cells should be able to use both our cells and the cells from the factory within a single design like a RISC-V CPU. Most of the necessary changes to the cells were made to make them compatible, but we havent tested the compatibility yet.
One interesting discovery was that the IHP cells seem to have some margin on the left and right side, which also gets added to our cells in the middle multiple times, so we might be able to shrink our cells a bit, but we have to investigate and try that.

Then I started to run the flow for the whole standard cell library with 656 cells, and we got a speed of approximately 2 of the most complex AOI cells per day, giving a rough estimation of one year to build a whole library on a single laptop. Luckily for our pad cell project we only need INV and NAND2 cells, which can be generated within an hour.
Later on it turned out that AAAAOI3332 (one of the most complex cells) takes more than a week to characterize:



Those complex cells aren't needed for the pad cells though that we are currently working on.

Originally we had planned to create both low and high voltage nfet/pfet models to work with StdCellLib/LibreCell, but it turned out that we only need the low voltage nfet/pfet models for the standard cells, and the voltage level shifting for high-voltage will be done with analog cells in the pad cells, not with standard cells. Therefore we only implemented the 1.8V low voltage nfet/pfet models in our standard cells for SG13G2.

What we delivered:
1) We refactored and brought the StdCell generator up to speed
1) Made the basic combinatoric logic for the pad cells work
2) Analog characterization of the cells allows for analog simulation of real world applications

During the work, we had a number of ideas for improvements in the future:

- Our Docker container could use a newer TCL version (>=9) for magic, there are some potential runtime issues with our older TCL Version (8.6 I think)
- The 3D visualisation of SG13G2 is missing the wells, we could add them (perhaps in a semi-transparent way?)
- We should define the pins for the power rails only on the top-most power rail layer
- **The vias of the power rails seem to be missing, we have to check that they are there**
- We could add support for 45° metal routing, which IHP is using. But this seems to be a huge project on its own.
- Reproducible builds (of standard cells) came up again, this time to verify the correctness of optimisations in the SPICE setup and parallelisation
- Support for asymmetric DRC rules in lclayout, preferably in a deterministic way
- We should test the interoperability of the our SG13G2 cells with the vendor cells
- We want to introduce a feature to automatically add a prefix and/or postfix to all the cell names of the generated cells, but we haven't decided yet, where in the flow that should be done exactly.
- lclayout has some empty net names that should be investigated
- We still get LVS errors in lclayout's internal LVS, which get ignored by our flow
- We currently only have lctime working, CharLib seems to have issues with the SG13G2 PDK and needs further investigation.
- One idea to improve the characterization speed is to implement a SPICE caching server
- Both CharLib and lctime are crashing reproducibly during the characterization of our cells