

LibreSilicon Standard Cell Library

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Abstract

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For further clarification consult the complete documentation of the process.

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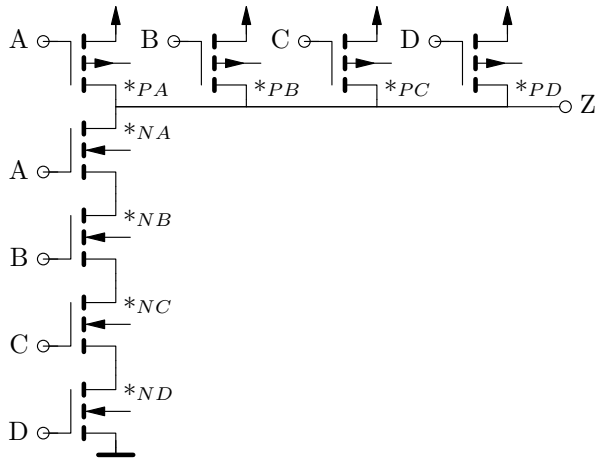
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1 Considerations

2 Logical Cells

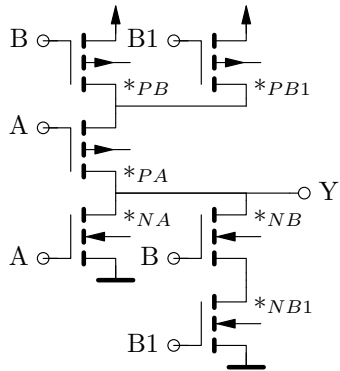
3 Cell AND4

Schematic (two stage, $1T_p/4T_n$ stacked, $10T$ total)



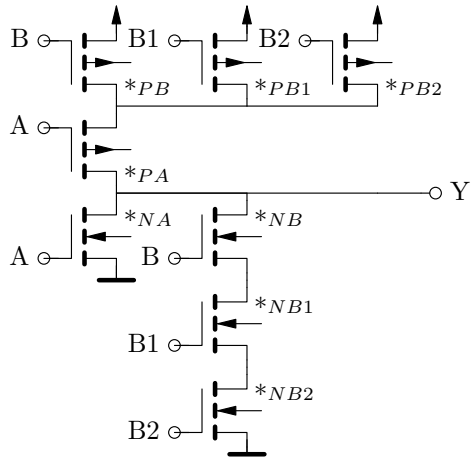
4 Cell AOI21

Schematic (one stage, $2T_p/2T_n$ stacked, $6T$ total)



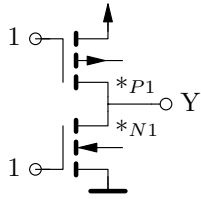
5 Cell AOI31

Schematic (one stage, $2T_p/3T_n$ stacked, $8T$ total)



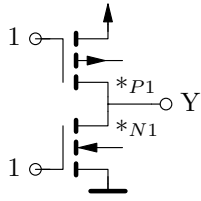
6 Cell BUFEX2

Schematic (one stage, $1T_p/1T_n$ stacked, $4T$ total)



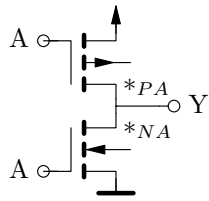
7 Cell BUFX4

Schematic (one stage, $1T_p/1T_n$ stacked, $6T$ total)



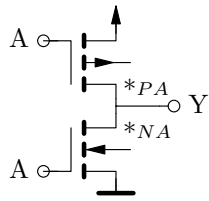
8 Cell INV

Schematic (one stage, $1T_p/1T_n$ stacked, $2T$ total)



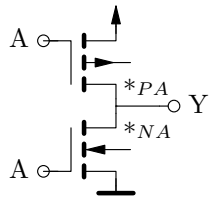
9 Cell INVX1

Schematic (one stage, $1T_p/1T_n$ stacked, $2T$ total)



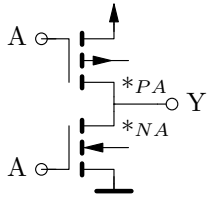
10 Cell INVX2

Schematic (one stage, $1T_p/1T_n$ stacked, $2T$ total)



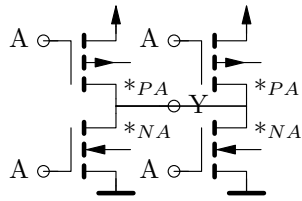
11 Cell INVX4

Schematic (one stage, $1T_p/1T_n$ stacked, $4T$ total)



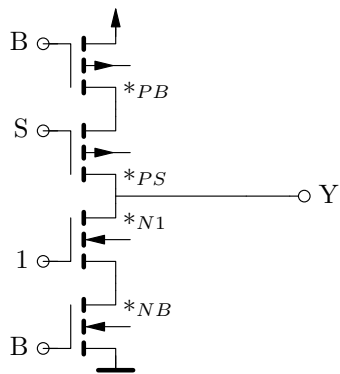
12 Cell INVX8

Schematic (one stage, $1T_p/1T_n$ stacked, $8T$ total)



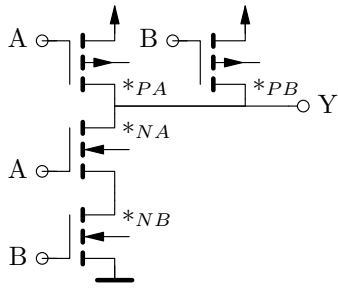
13 Cell MUX2X1

Schematic (one stage, $2T_p/2T_n$ stacked, $10T$ total)



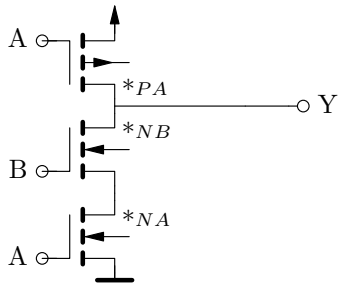
14 Cell NAND2

Schematic (one stage, $1T_p/2T_n$ stacked, $4T$ total)



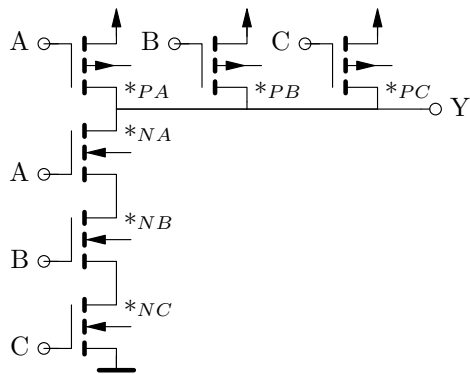
15 Cell NAND2X1

Schematic (one stage, $1T_p/2T_n$ stacked, $4T$ total)



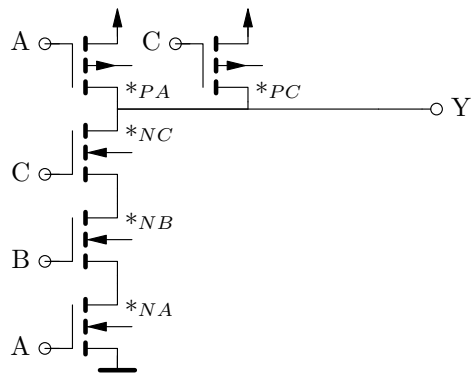
16 Cell NAND3

Schematic (one stage, $1T_p/3T_n$ stacked, $6T$ total)



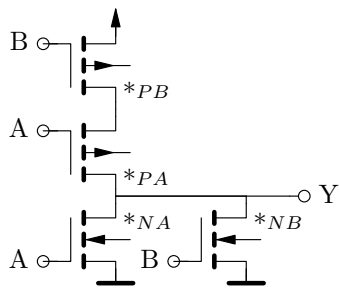
17 Cell NAND3X1

Schematic (one stage, $1T_p/3T_n$ stacked, $6T$ total)



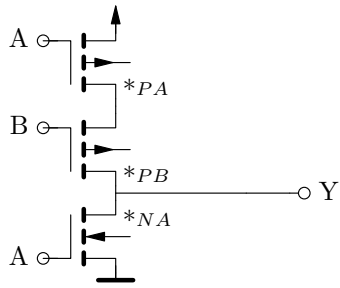
18 Cell NOR2

Schematic (one stage, $2T_p/1T_n$ stacked, $4T$ total)



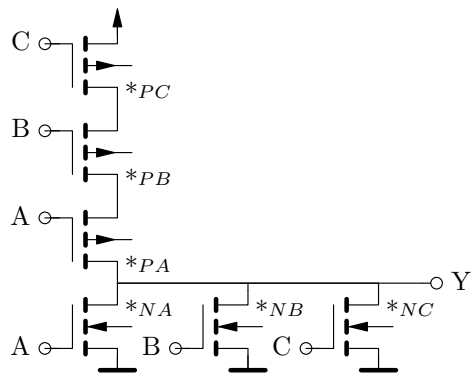
19 Cell NOR2X1

Schematic (one stage, $2T_p/1T_n$ stacked, $4T$ total)



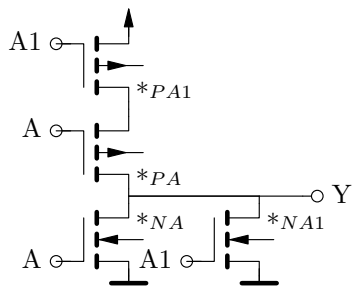
20 Cell NOR3

Schematic (one stage, $3T_p/1T_n$ stacked, $6T$ total)



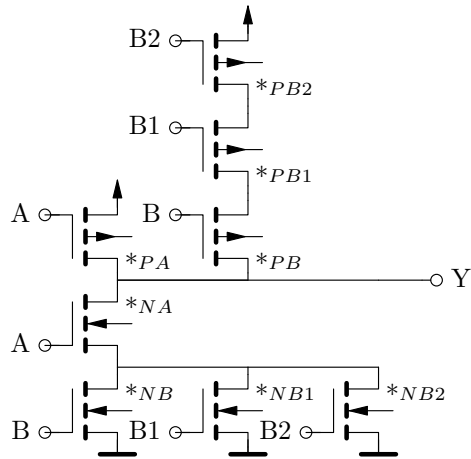
21 Cell OAI21

Schematic (one stage, $2T_p/1T_n$ stacked, $4T$ total)



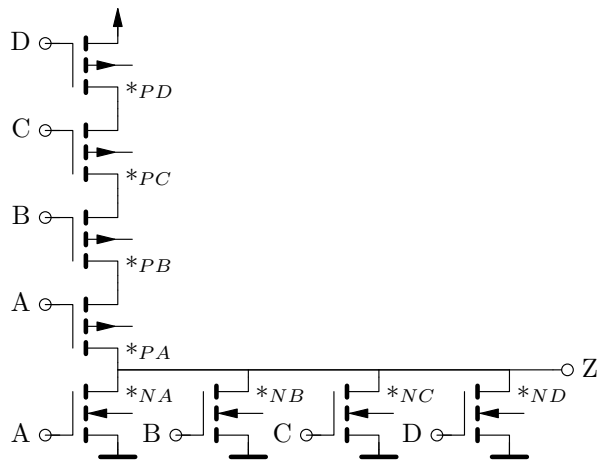
22 Cell OAI31

Schematic (one stage, $3T_p/2T_n$ stacked, $8T$ total)



23 Cell OR4

Schematic (two stage, $4T_p/1T_n$ stacked, $10T$ total)



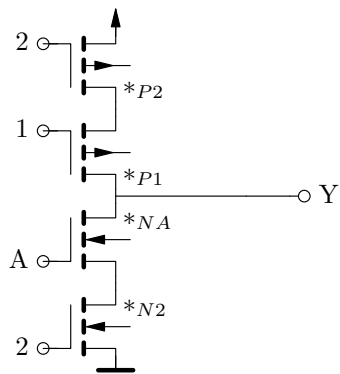
24 Cell TBUF_{X1}

Schematic (one stage, $1T_p/1T_n$ stacked, $6T$ total)

—○ vdd

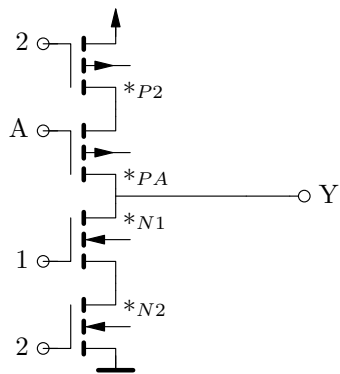
25 Cell XNOR2X1

Schematic (one stage, $2T_p/2T_n$ stacked, $12T$ total)



26 Cell XOR2X1

Schematic (one stage, $2T_p/2T_n$ stacked, $12T$ total)



VDDIO
GND
ANA

